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Formation of Low-Resistivity Gate Electrode Suitable for the Future Devices Using Clustered DCS-Wsix Polycide

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1. Introduction

The first motivations for running the integrated cluster process of WSix polycide (***Cluster***) as a gate electrode, instead of the conventional polycide (***Control***), are process simplification and defect density reduction. The Cluster is defined as the sequential deposition of *in-situ* doped poly-Si and dichlorosilane based CVD tungsten silicide (DCS-WSi_X) without vacuum break. However, it was found that the deposition resulted in the formation of W-excessive layer at the WSix/poly-Si interface, which might cause defect generation [1]. To solve this problem, a capping layer using undoped poly-Si prior to the DCS-WSix deposition was suggested [2]. Second, the minimum resistivity of DCS-WSix is known to be around 100 $\mu\Omega\cdot$cm after annealing, which is too high for the polycide to be used as a gate electrode. Therefore, one of the fundamental concerns in the cluster process is the reduction of its resistivity. This paper describes a new technique satisfying the above criteria using amorphization and recrystallization of DCS-WSix.

2. Experimental Procedure

The polycides shown in Fig. 1 were formed using an Applied Materials CENTURA cluster platform. P (50keV), As (70keV), B (20keV), or Ar (70keV) were implanted (***Imp***) with varying dose from 1×10^{15} to $8\times10^{15}cm^{-2}$, in which the energy was calculated by TRIM simulator. In case of the Cluster-2, WSix(150nm), the energy of P was adjusted to be 80keV. Recrystallization was performed by annealing at 900 ℃. The properties were evaluated using a 4-point probe, XRD, SEM, and TEM. A 0.25 μm CMOS was fabricated using a conventional fabrication process except the formation of the gate electrode shown in Fig. 1.

3. Results and Discussion

For comparison, the structure of the Control before and after annealing is shown in Fig. 2. The as-deposited and the annealed films show a feather fine and a polycrystalline structure having 20-60 nm in diameter, in which the resistivities are 900 and 90 $\mu\Omega\cdot$cm, respectively.

Fig. 3 compares XRD of 100nm thick WSi_X, before and after Imp, in which the dose was fixed at $5\times10^{15}cm^{-2}$. As-deposited film showed a hexagonal WSi_2 (H-WSi_2). However, the Imp. reduced the peak intensities, and amorphized the film, especially in case of P and Ar Imp, as shown in Fig. 4(a, b). And such an amorphization results in the reduction of WSix's Rs, as shown in Fig, 4(c).

The annealing resulted in the recrystallization, yielding a large-sized tetragonal WSi_2 (T-WSi_2) [Fig. 5(a)]. In case of P Imp, Rs was decreased with increasing the dose [Fig. 5(b)]. Specifically, in case of *Cluster-2*, the Rs is further decreased, and the resistivity is monitored about 65 $\mu\Omega\cdot$cm, which is about 30% lower than that of the *Control*. This comes from the formation of large-sized grains due to the amorphization and recrystallization. In case of the other Imp, however, Rs shows less dependence or rather increased with the dose, which is found to be due to the formation of a compound (for As) and a void (for Ar), as indicated by arrows in Fig. 6. This means that P is the best Imp agents for reducing Rs of the WSix polycide.

To further reduction of gate Rs, a simple increase of the WSix thickness could be suggested with fixing the total thickness, "*Cluster-2*" noted in Fig. 1. Although this decreases the line Rs [Fig. 8], the gate degradation such as V_T shift and dopant depletion effect is observed [Fig. 7(a)]. However, P Imp. into cluster-2, *Cluster-2, P (80keV)*, results in the improvement of the dopant loss as well as the gate oxide reliability, TDDB [Fig. 7(b)]; in fact, C_{INV}/C_{ACC} of the Cluster-2, P(80keV) and the Control were measured to be 0.998 and 0.932, respectively.

Fig. 8 shows the Rs dependences on the line width. Because of the above effects, thinner WSix with P Imp, *Cluster-1, P(50keV)*, shows nearly the same Rs as that of thicker WSix, *Cluster-2*. Similarly, it was exhibited that the P Imp on the thicker WSix, *Cluster-2, P(80keV)*, reduced the Rs and improved its uniformity. Meanwhile, the device performance of *Cluster-2, P(80keV)* was evaluated to be the same as that of the *Control*, as shown in Figs. 9 and 10.

4. Conclusion and Summary

P was found to be the best implantation agent for the amorphization of WSix and the reduction of film resistivity. About 30% of WSix's resistivity was decreased by the P implantation. Also, the P improved the dopant loss and the reliability of gate electrode. As a result, its application to CMOS revealed better qualities as a gate electrode, while having the same device performance as that of the conventional WSix polycide.

Acknowledgments

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References

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2) J.S. Byun, B.H. Lee, J.S. Park, and J.J. Kim, J. Electrochem. Soc. Submitted.

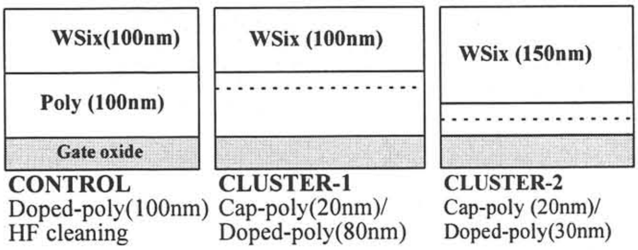

Fig.1. Cross-sectional schematics of splits.

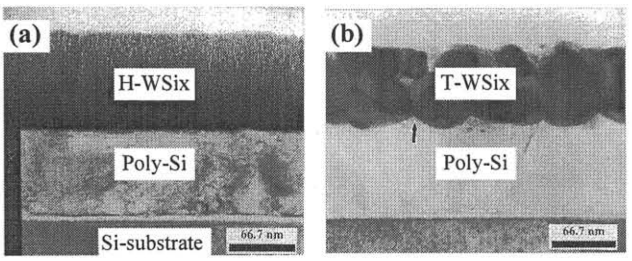

Fig. 2. XTEM of the Control WSix polycide : (a) as-deposited and (b) after annealing at 900 ℃ for 30 min.

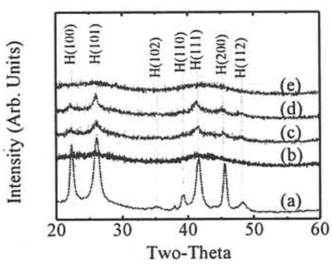

Fig. 3. XRD spectra of Cluster-1 : (a) as-deposited, and after (b) P, (c) As, (d) B, and (e) Ar implantation.

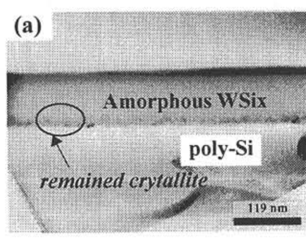

Fig. 4(a). XTEM of P ($5 \times 10^{15}cm^{-2}$, 50keV) implanted polycide

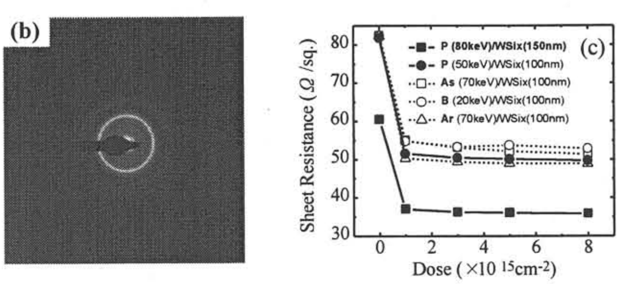

Fig. 4. (b) Diffraction pattern obtained from Fig. 4(a), proving the amorphous crystallinity of the WSix layer. (c) Rs variation of implanted films as a function of implantation condition.

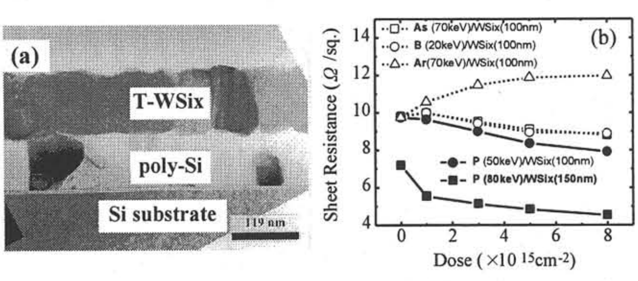

Fig. 5. (a) XTEM of the P implanted film after annealing, showing the large-grain sized WSix. (b) Rs variation of annealed film as a function of implant condition.

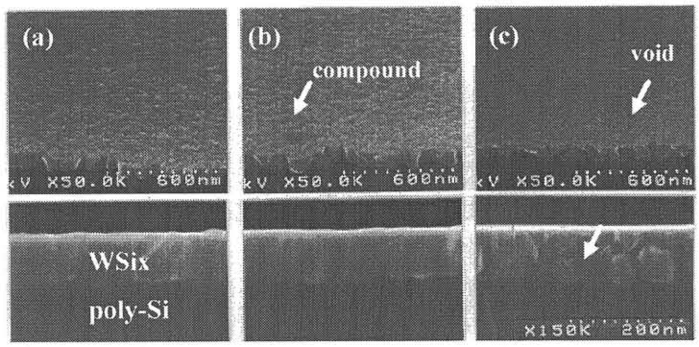

Fig. 6. Tilted and cross-sectional view of the film after annealing : the amorphization was performed by (a) P, (b) As, and (c) Ar implantation.

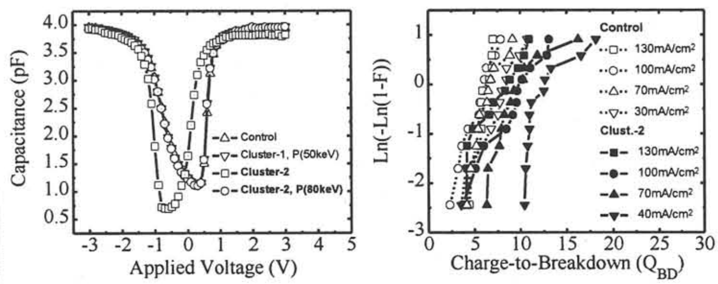

Fig. 7. (a) Quasi-static CV and (b) TDDB characteristics of the split.

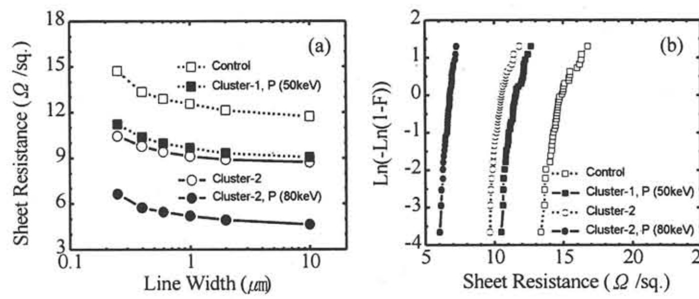

Fig. 8. (a) Line Rs variation as a function of line width, and (b) Rs distribution at 0.25 μm line width.

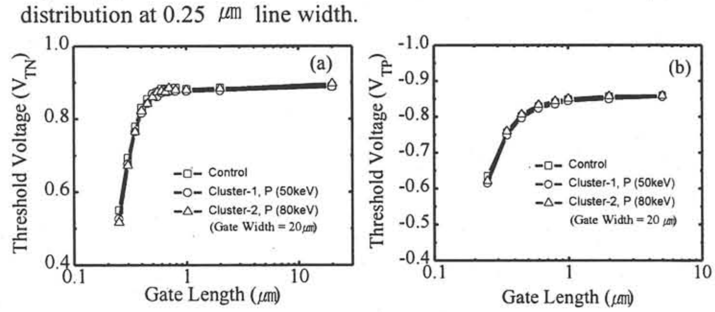

Fig. 9. Threshold variation of (a) NMOS and (b) PMOS.

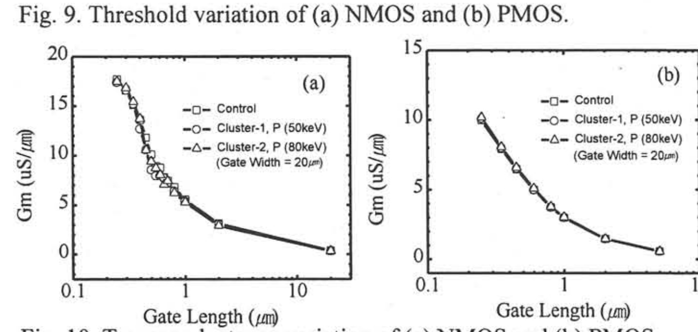

Fig. 10. Transconductance variation of (a) NMOS and (b) PMOS.