Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 286-287

W-Plug Common Contact with $CoSi_2$ Ohmic Layer for Scaled DRAM and Merged DRAM in Logic (MDL) Devices

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1. Introduction

As the design rule of scaled DRAM and Merged DRAM in Logic(MDL) devices enters into the Giga bit era, several key technologies, such as Shallow Trench Isolation(STI), high dielectric capacitor and planarization over capacitor have been developed[1]. The application of Damascene W BL Common contact(DWBC) process, as shown Fig.1, has advantages on the improvement of device speed due to low sheet resistance of W BL(~2 Ω/sq.) and effectiveness on circuit layout from the capability of making both P^+ & N^+ contacts. Furthermore, dual-damascene BL process provides significant improvements in DOF margin for all the subsequent lithographic steps which are inevitable in scaled and MDL devices for next generation and W BL landing pad can avoid the difficulty of deep metal contact formation. DWBC process, however, has considerable issue on BL to active P^+ contact resistance(Rc) under high thermal budget produced during the formation of capacitor in the Capacitor Over BL(COB) structure. Increasement of P^+ Rc with thermal budget, is believed mainly due to the rapid reduction of dopant(B^+) concentration in P^+ region by forming compound(TiB_2) with either Ti or $TiSi_2$ layer at the contact bottom. Therefore, $CoSi_2$ ohmic layer known to form no boride compounds is applied to investigate the behavior of P^+ Rc under high thermal budget.

2. Experimental

Either $TiSi_2$ or $CoSi_2$ ohmic layer on contact bottom was formed by silicidation process, and depositions of TiN barrier and blanket W followed. Tungsten Chemical Mechanical Polishing(CMP) was then employed and capacitor process(above 800℃, 30min.) was carried out. Electrical and analytic measurements were performed using the 256M DRAM device.

3. Results and Discussion

W BL to active Rc in P^+ and N^+ areas with $TiSi_2$ and $CoSi_2$ layers are shown in Fig.2. P+ Rc at 0.4*0.4 μm contact size is shown above 3000 Ω/cnt, which was ~500 Ω/cnt before capacitor process. Process optimization[2] using plug implantation, activation, RF contact cleaning and thickness of Ti on DWBC can reduce P^+ Rc increasement, but it has a limitation that Rc is decreased around 2000 Ω/cnt. Application of $CoSi_2$ ohmic layer, however, clearly presents P^+ Rc, below 1000 Ω/cnt with very narrow distribution. N^+ Rc, ~200 Ω/cnt, in Fig.2 (b) with $TiSi_2$ and $CoSi_2$ layers shows no differences because no compound can be formed between either silicide and dopant As. The reason of P^+ Rc increasements in $TiSi_2$ layer with thermal budget is turned out to be rapid consumption of B due to TiB_2 formation at the interface between $TiSi_2$ and B-doped Si. SIMS analyses in Fig.3 (a) and (b), were obtained from the samples with $TiSi_2$ and $CoSi_2$ layer after heat treatments (800℃, 60min.), respectively. B redistribution in the sample with $TiSi_2$ layer shows high solubility in $TiSi_2$ and "long tail" parallel to the corresponding Ti signal, caused by the hardness of existing TiB_2[3]. On the other hand, B concentration in Fig.3(b) represents low B solublity in $CoSi_2$ and no borides formed at the interface. This behaviors of B dopant in both silicides explains the P^+ Rc variations under high thermal budget. Figure 4 presents median P^+ Rc at different contact sizes and its variation in $CoSi_2$ layer is significantly smaller than that in $TiSi_2$ layer, which will be crucial on the contact process into future scaled devices. TEM micrographs at the contact bottom show (a) $TiSi_2$ and (b) $CoSi_2$ layers in Fig.5. Formation of silicide is influenced by the residues remained at the contact bottom because only HF-based wet cleaning is used without in-situ RF cleaning before the deposition of either Ti or Co. It is known that titanium has an ability to dissociate the trace of native oxide and polymers, but Co has not. Compared to agglomerated $TiSi_2$ layer, ~250 Å, formed continuously, $CoSi_2$ shows discontinuous grain-type layer with the thickness of ~400 Å. It is because the area of $CoSi_2$ reaction is believed to be restricted depending upon the cleanness of contact bottom. This grain-type of $CoSi_2$ formation causes 2 order higher N^+ contact leakage current than that of the other in Fig.6.

4. Conclusion

The abrupt increasement of P^+ Rc during the subsequent high thermal cycling for capacitor formation has been effectively treated and reduced below 1000 Ω/cnt by the application of $CoSi_2$ ohmic layer on DWBC process. Feasibility of $CoSi_2$ layer in small contact size (<0.35 μm) promises its implement in the future scaled DRAM and MDL devices.

References

1) S.P.Sim et al.:IEDM,1996,p597
2) S.Choi:(private communication)
3) V.Probst et al.:Appl.Phys.Lett,52(1988),p1803

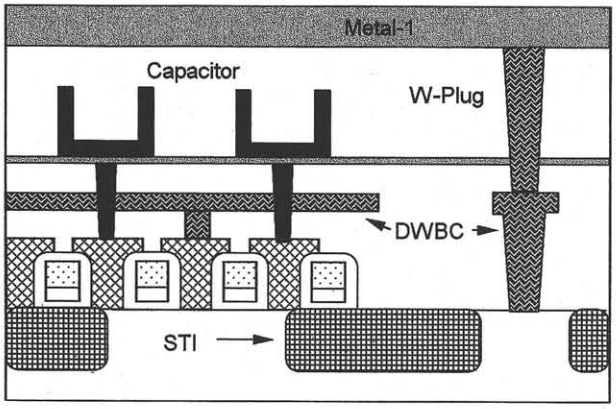


Fig.1 Schematic vertical view of DRAM with DWBC process

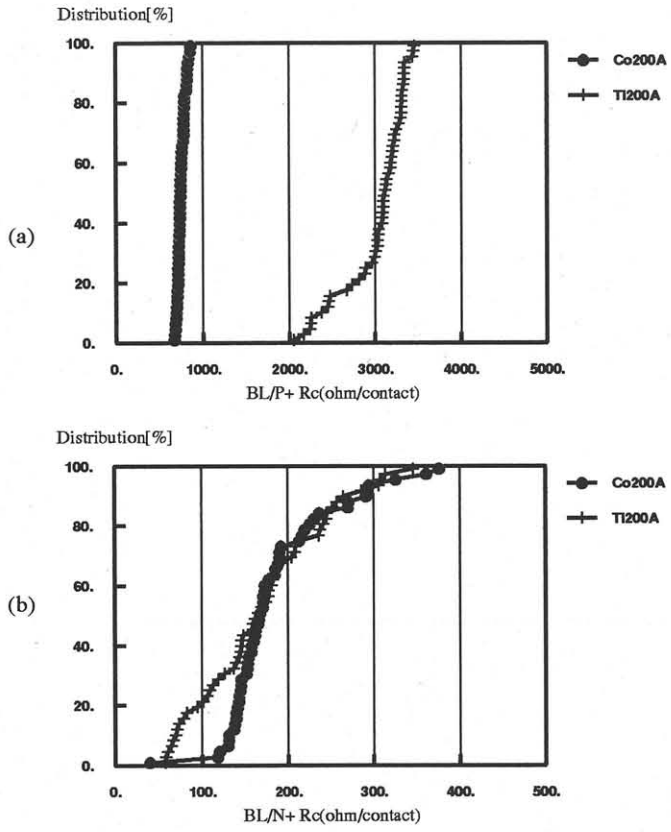
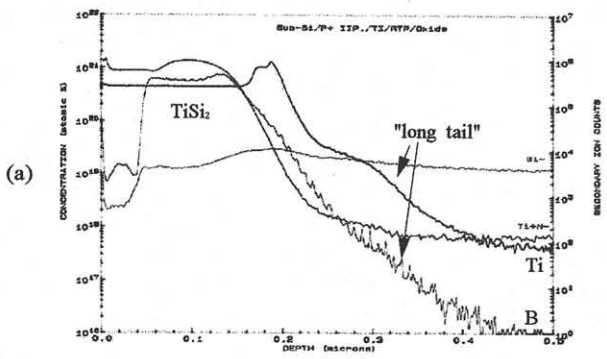


Fig.2 Rc distributions of (a)BL/P$^+$ & (b)BL/N$^+$ using $TiSi_2$ & $CoSi_2$ ohmic layers



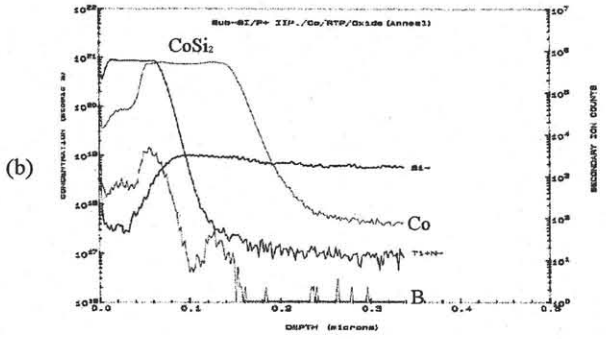


Fig.3 SIMS depth profile across (a)$TiSi_2$ & (b)$CoSi_2$ layer/ B-doped Si after thermal cycle(800℃, 60min.)

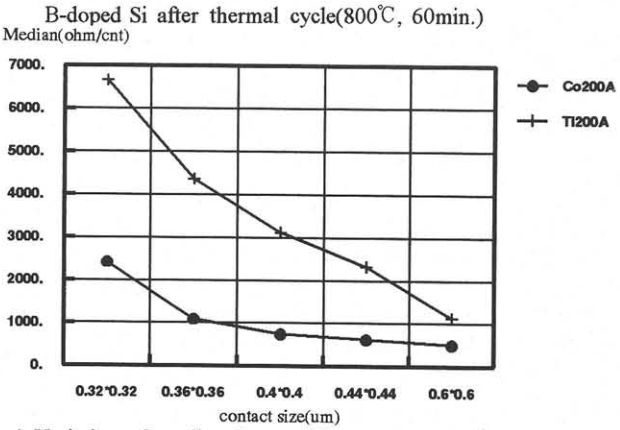


Fig.4 Variation of median Rc at different sizes of P$^+$ contact

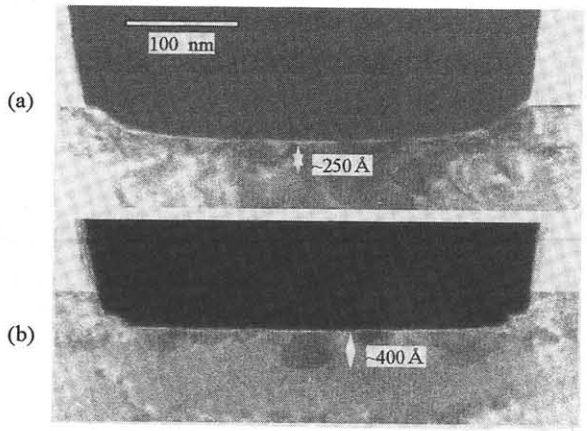


Fig.5 TEM micrographs of (a)$TiSi_2$ & (b)$CoSi_2$ layers at the bottom of BL/P$^+$ contact

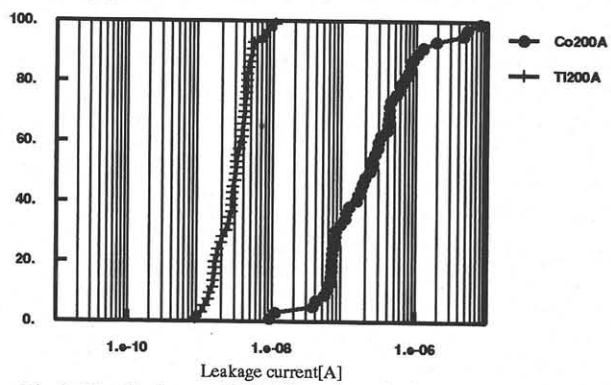


Fig.6 Distributions of BL/N$^+$ contact leakage current