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A Reliable Double Level Interconnection Technology for Giga Bit DRAMs Using SiO_2 Mask Al Etching and PECVD SiOF

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1. Introduction

A reliable fabrication technology for scaled down Al interconnection over a large vertical step is a key to realize giga bit DRAMs with stack capacitor, since the lithography and the etching for Al become difficult due to the large step between memory cell and peripheral circuit area. Conventional Al etching using photoresist(PR) mask need a thick PR, due to the low etching selectivity to Al. Lithography of fine patterns is difficult over the large step area especially in the case of using thick PR. Another issue is a gap filling of Al interconnection with the minimum space below 0.35 μm size. Conventional PECVD SiO2 cannot fill such small spaces.

In this paper, a SiO2 mask etching process has been applied to form Al interconnection with the width as small as 0.35μm over large step(1 μm). The SiO2 doesn't need to use a thick PR for the patterning, and the Al etching selectivity is higher than PR. A PECVD SiOF, which has a better gap filling property than the PECVD SiO2, has been applied to fill the space down to 0.2 μm(AR≒2), combined with a tapered Al structure formed by the SiO2 mask etching. Finally, double level interconnection with 0.3 μm via have been fabricated using the technology.

2. SiO2 mask etch for Al interconnection

Figure 1 shows schematic cross section of our giga bit DRAMs interconnection system. The step height is about 1 μm. The Al interconnections were fabricated over 1 μm step using a SiO2 mask or a conventional PR mask. The interconnection structure is a TiN/ 400nmAlCu/ 100nmTiN/ 50nmTi deposited by sputtering. The 200nm thick SiO2 mask was deposited by PECVD. The line width is between 0.3 to 0.8 μm. The yield of the interconnection was improved drastically by the SiO2 mask process compared to the PR mask process as shown in Figure 2. Figure 3 shows the SEM micrograph of the Al interconnection on a DRAM structure with a 1 μm step using the SiO2 mask, indicating excellent Al patterning both on the cell area and the peripheral circuit area compared to that of the PR mask as shown in Figure 4. The difference is due to the Al etching selectivity and the PR thickness which determines the focus margin and the resolution in lithography. Table 1 shows the Al etching selectivity and the PR thickness used for the process.

3. 0.2 μm Gap fill by PECVD SiOF combined with tapered Al structure

A tapered Al interconnection structure can be fabricated using the SiO2 mask etching. Figure 5 shows the cross sectional view of 0.3 μm Al interconnection. This structure is formed by side wall deposition during the Al etching using Cl2/N2/BCl3 gas chemistry[1]. The tapered structure is effective to improve the gap filling property, especially combined with PECVD SiOF (ASMJ;EAGLE-10). The PECVD SiOF has an improved gap filling property due to etching the deposited SiOF film on the shoulder of Al pattern[2,3]. It was determined that 5 atom % fluorine(F) conc.of SiOF film ($\varepsilon \fallingdotseq 3.9$) is good for the gap filling from the result of gap filling dependence on the flow rate as shown in Figure 6. This figure shows minimum gap filling ability of Al interconnection space form 0.2 to 1.50 μm.

Figure 7 and Table 2 shows a comparison of gap filling performance for 0.2 to 1.50 μm spaces. Both the PECVD SiOF and the SiO2 mask process are necessary to fill 0.20 μm space(AR≒2).

4. Integration

Double level interconnections with tungsten(W) vias was fabricated using the described technology. Figure 8 shows the schematic cross section of the structure. Figure 9 shows the following process sequence. 1)1st Al interconnection patterning and etching using the SiO2 mask. 2) PECVD SiOF and SiO2 deposition. 3)SOG and etchback planarization. 4)blanket W filling and etchback for via formation 5) 2nd Al interconnection formation.

The PECVD SiO2 layer in the 2nd step is protected to absorption in SiOF. The increase of dielectric constant for absorption is not seen in the deposited SiO2 on SiOF, as shown in Figure 10.

Figure 11 shows the via resistance and their yield. A 100% yield was obtained for the all via sizes. It was also confirmed that the property was stable after 450℃ anneal. The results indicate that reliability of the developed technology.

5. Conclusion

The double level interconnection technology for giga bit DRAMs with a large vertical step and the minimum line space of 0.35 μm has been proposed. The SiO2 mask process improved the yield of Al interconnection over the 1 μm step. The 0.2 μm space(AR≒2) was filled by the PECVD SiOF, combined with the tapered Al interconnection structure formed by the Al etching using the SiO2 mask. The double level interconnection with the minimum via size of 0.3 μm was fabricated. A 100% yield was obtained with the via both before and after the 450℃ anneal. This technology is promising for giga bit level DRAMs.

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Reference

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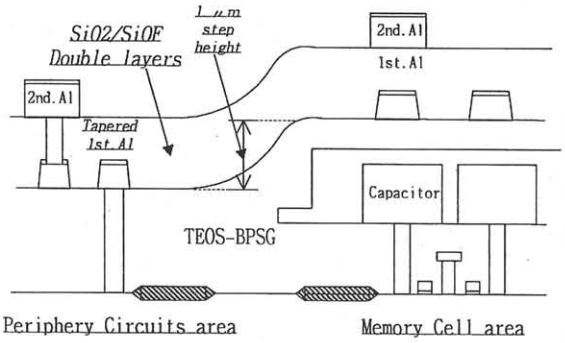


Figure 1 Schematic cross section of a giga bit DRAM interconnection system

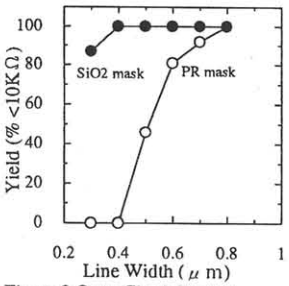


Figure 2 Open Check Results
●:Using SiO2 mask;○Using PR mask
Step height is 1 μm

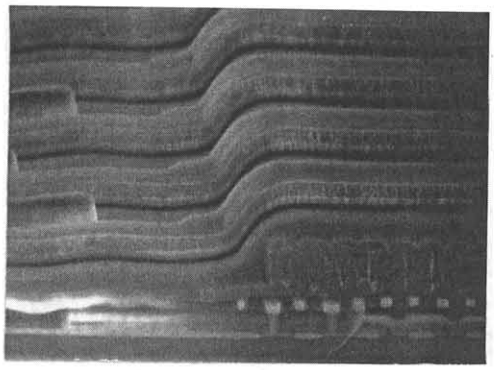


Figure 3 SEM micrograph of the Al interconnection formed using SiO2 mask

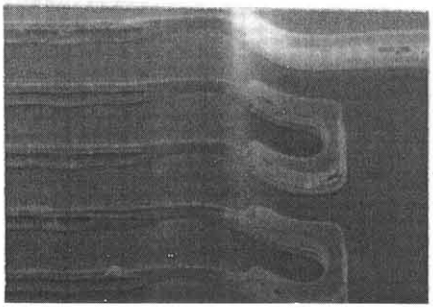


Figure 4 SEM micrograph of the Al interconnection formed using PR mask

Table 1 Comparison of the photoresist thickness and Al etching selectivity between SiO2 mask etch and a conventional PR mask etch

	SiO2 mask	PR mask
Photoresist thickness	700nm	1,700nm
Al etching selectivity	10	3

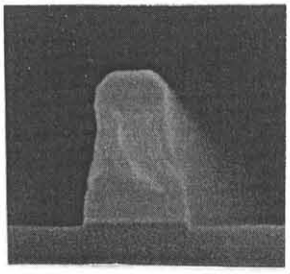


Figure 5 Tapered Al interconnection structure using SiO2 mask ; 0.30 μm line

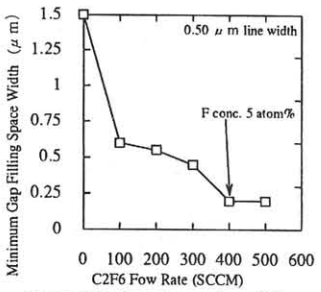
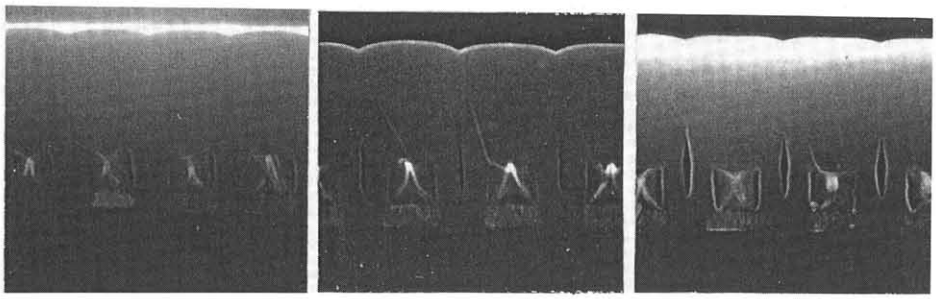


Figure 6 The dependence of gap filling property on F souse gas flow rate



(a)SiO2 mask + PECVD SiOF (b)SiO2 mask + PECVD SiO2 (C)PR mask + PECVD SiOF

Figure 7 Comparison of gap fill performance (a)SiO2 mask + PECVD SiOF(b)SiO2 mask + PECVD SiO2(C)PR mask + PECVD SiOF ;ILD thickness:1 μm; (a)L/S=0.50/0.20 μm(AR≒2.0)(b), (c)L/S=0.50/0.35(AR≒1.7)

Table 2 Comparison of gap fill performance

	SiOF ILD		SiO2 ILD
Space Width	SiO2 mask	PR mask	SiO2 mask
0.20 μm	○	×	×
0.25 μm	○	×	×
0.30 μm	○	×	×
0.35 μm	○	×	×
0.40 μm	○	×	×
0.50 μm	○	×	×
0.70 μm	○	×	×
1.50 μm	○	○	○

○:Good ×:Poor ; Al wires height:400nm

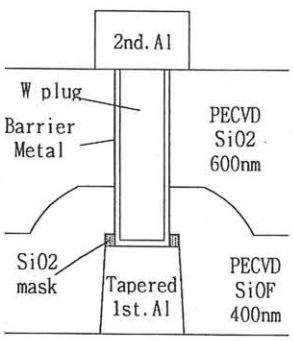


Figure 8 Schematic cross section for double level interconnection

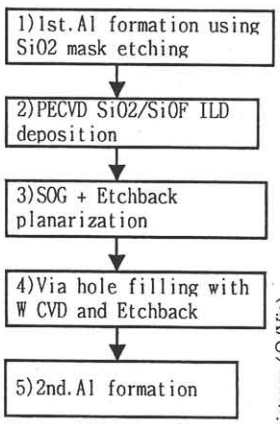


Figure 9 Fabrication sequence for the double level interconnection

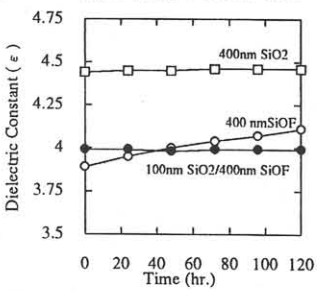


Figure 10 Comparison of dielectric constant stability between a SiO2/SiOF ILD and SiOF ILD
□:400nm SiO2;○:400nm SiOF
●:100nm SiO2/400nm SiOF

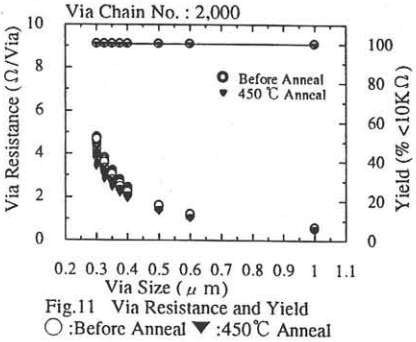


Fig.11 Via Resistance and Yield
○ :Before Anneal ▼ :450℃ Anneal