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# Directional Plasma CVD Technology for Sub-Quarter Micrometer Feature Size Multilevel Interconnection

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## 1. Introduction

Low-parasitic-capacitance, highly packed multilevel interconnections are necessary to improve the operating speed in high speed ULSIs. Interlevel dielectrics (ILDs) using organic spin-on material, especially spin-on-glass (SOG), are considered to be the most promising materials for achieving this, since they have an excellent gap-filling capability and their permittivity is below 3[1]. Also, organic SOG can be globally planarized by a selective chemical mechanical polishing (CMP)[2]. The performance of the ILD using the process has already been shown in that their parasitic capacitance between metal lines is reduced to about 70% of that of conventional structures[1].

The ILDs using organic SOG, however, usually need a liner layer, e.g., a plasma enhanced CVD $SiO_2$ (PECVD) layer, for adhesion and metal-line passivation. The liner layer is considered a major limiting factor of ILDs application to quarter-micrometer feature-size interconnections or below due to its insufficient step coverage or poor film quality.

We have developed a directional plasma CVD technology (DPCVD) that makes improved film coverage profiles and film quality attainable. This paper describes the features of the DPCVD and its application to the fabrication of quarter-micrometer feature-size multilevel interconnections.

## 2. Experimental

*Interconnection using organic SOG*

Fig 1 shows the interconnection cross section using SOG. The metal lines, consisting of a barrier and an Al alloy layer and patterned according to a $SiO_2$ mask, are covered with a $SiO_2$ liner layer deposited by PECVD or by the DPCVD. An organic SOG, HSG R7 (HSG2209S R7; Hitachi Chemical, Co.), is coated onto the surface to fill the gaps, and globally planarized by the CMP. On the surface, PECVD $SiO_2$ capping layer is deposited, and via holes with CVD W plugs are formed.

When the PECVD liner layer is thick, the parasitic capacitance between the metal-lines is not lowered, since most of the space is occupied by the liner layer, though the process is easy to control because the end point of the CMP is easily determined. To reduce the capacitance, the lateral ledge of the $SiO_2$ liner has to be made narrower by using thinner liner. However, to fabricate such a structure requires rather delicate process control, especially in determining the end point for the SOG CMP, as shown in Fig. 1(a).

On the other hand, the DPCVD technology deposits a thick $SiO_2$ layer only on top of the metal-lines, while depositing a thin high-quality layer on the side walls. The DPCVD liner film makes the CMP process much easier to control, without increasing the parasitic capacitance.

*Deposition System and Source Gas*

We used a parallel-plate, wide-gap-electrode, bias-plasma CVD system (Fig. 2). The prime objective in DPCVD is to realize directional step coverage, rather than gap-filling as in other plasma CVD techniques. For this reason, we used only reaction gases; that is a mixture of either triethoxysilane (TRIES) or tetraethoxysilane (TEOS) with oxygen, without including inert gases such as Ar that are usually added for gap-filling and planarization. Table 1 shows the process parameters[3].

*Step Coverage and Film Characteristics*

We evaluated the step coverage by using a parameter, "opening width," i.e., the width of the liner space between metal lines. The films were characterized through measurement of the refractive index, stress, and etching rate.

## 3. Results and discussion

Figure 3 shows the deposition rate dependence on biasing. Little reduction in the deposition rate by substrate biasing occurred when the pressure was 0.5 Torr or higher, showing that there was little resputtering in that pressure range. The influence of the substrate biasing on the film profile is shown in Fig. 4. The TRIES-based $SiO_2$ film deposited under high pressure (4 Torr) and 600 W biasing, had significantly improved step coverage and film quality, i.e., a much narrower lateral-ledge on metal-line side walls. The ratio of lateral-ledge width to nominal thickness and the etching rate of the layer on metal-line side walls were reduced to less than 60% and 50%, respectively, of those with conventional PECVD.

Figure 5 shows the opening width dependence on the pressure and source gas. These results suggest that the TRIES-based $SiO_2$ films will be able to provide a sufficiently wide opening for metal lines with spacing below $0.2\mu$m. A cross section of a three-level interconnection using a DPCVD $SiO_2$ film is shown in Fig. 6. The parasitic capacitance of the test device was reduced to 70 - 80 % of that of conventional structure using the liner layer of the same nominal thickness of $0.2\mu$m. The low-parasitic-capacitance structure was obtained under a very easy process control. The DPCVD technology is clearly very promising also for use in the fabrication of ILDs using inorganic SOGs.

## 4. Conclusions

Directional plasma CVD technology, which is suitable for application to SOG-ILDs, makes it possible to deposit thick $SiO_2$ films on metal lines, while also depositing very thin high quality films on the side walls, resulting in a reduced parasitic capacitance. We expect the DPCVD technology to be very effective for forming high-

performance low permittivity ILDs in high-speed ULSIs.

## References


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2] Y. Homma, T. Furusawa, K. Kusukawa, M. Nagasawa, Y. Nakamura, M. Saitou, H. Morishima, and H. Sato, *Proc. VMIC, Santa Clara* (1995) p.457.
3] M. Saitoh, Y. Kudoh, Y. Homma, Ext. Abst. 43rd Spring Meeting, J. Soc. Appl. Phys., No.26a-N-9, 1996.


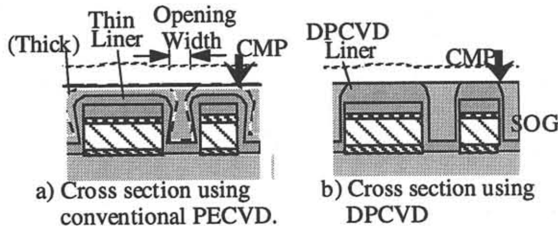


Fig 1. Comparison of interconnection structure using SOG.

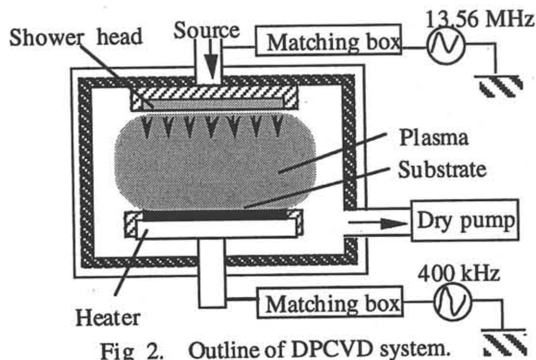


Fig 2. Outline of DPCVD system.

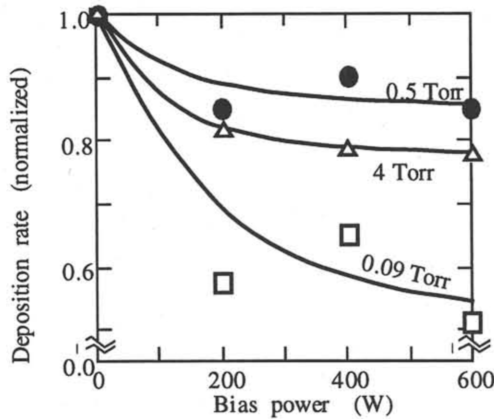


Fig 3. Deposition rate vs. Bias power.

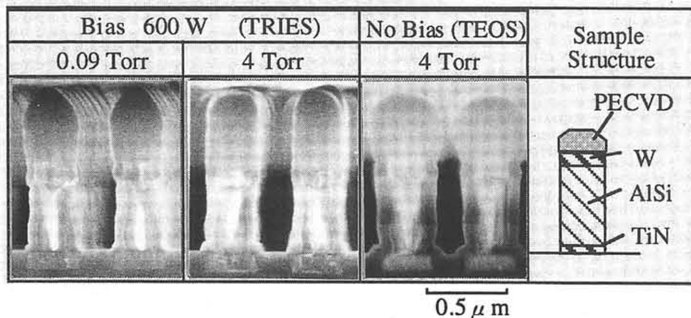


Fig 4. Step-coverage of SiO2 liner films

Table 1. Process parameters

| Source gas | TRIES, TEOS (max. 100 sccm) |
|---|---|
| Oxydation gas | O2 (max. 900 sccm) |
| Pressure | 0.09 to 4 Torr |
| Temperature | 360℃ |
| RF Power (13.56 MHz) | 300 W |
| Bias Power (400 kHz) | 0 to 600 W |
| Electrode gap | 5 to 20 mm |

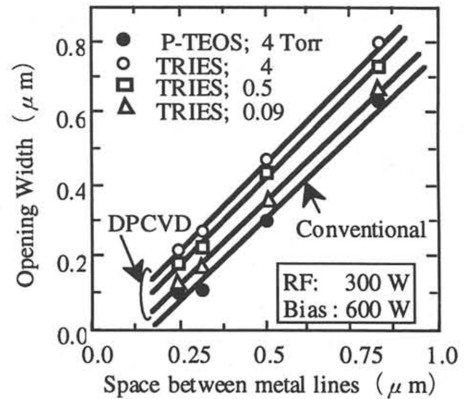


Fig 5. Opening width dependence on deposition conditions.

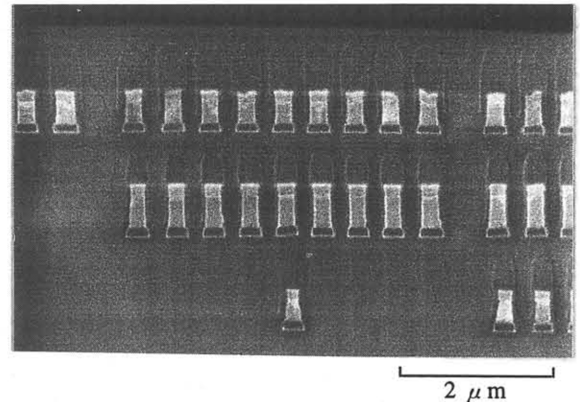


Fig 6. Cross section of 3 level interconnection using the DPCVD SiO2 film.

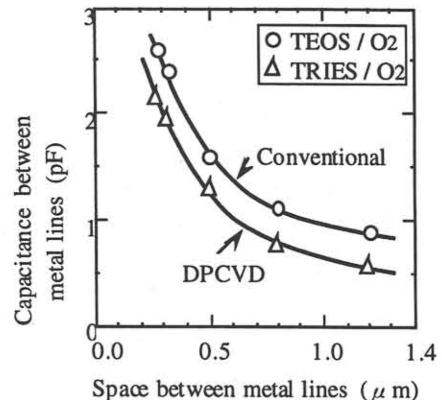


Fig 7. Comparison of parasitic capacitance.