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Highly Reliable Interpoly Oxide Using ECR N_2O-Plasma for Next Generation Flash Memory

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1. Introduction

High quality interpoly dielectric is required to improve data retention characteristics in nonvolatile memories [1]. Although stacked ONO structure is widely used, it suffers from its thickness scaling limitation, high process temperature, and degradation of tunnel oxide due to Si_3N_4 stress [1],[2]. Moreover, polyoxide on $POCl_3$ doped poly-Si has poor electrical properties due to its rough polyoxide/poly-Si interface [3]. Thus, research on high-quality low-stress thin polyoxide on doped poly-Si is greatly needed. In this paper, we present low temperature N_2O-plasma oxide grown on *in-situ* doped poly-Si to improve surface roughness and long term reliability.

2. Experiments

To investigate the electrical characteristics of N_2O-plasma polyoxide, capacitors with n^+-poly-Si floating gate/oxide/n^+-poly-Si control gate structure were fabricated. *In-situ* doped a-Si film of 100nm thickness for the floating gate electrode was deposited using SiH_4 and PH_3 and annealed at 900℃. Then, ECR N_2O-plasma polyoxide of 12nm thickness was prepared at 400℃, 1.4mtorr and 600W. Control thermal polyoxide was also grown at 850℃ in dry O_2 ambient. After the control gate electrode of 300nm was patterned, aluminum contacts were opened on both the n^+-poly-Si gates and annealed at 400℃ in 10% H_2/N_2.

3. Results and Discussion

Fig. 1 shows J-E curves of thermal polyoxide and N_2O-plasma polyoxide and Fig. 2 shows their cumulative breakdown field. N_2O-plasma polyoxide has lower leakage current, higher breakdown field, and better polarity-independence, which reveals that its bulk property and interface roughness are superior to those of thermal oxide.

To investigate the surface morphology of poly-Si film, AFM measurements were performed. Fig. 3 shows the AFM images of poly-Si film before oxidation, after thermal oxidation, and after ECR N_2O-plasma oxidation and corresponding rms value of roughness are 6.4nm, 9.6nm, and 4.6nm, respectively. N_2O-plasma oxidation does not degrade surface roughness of poly-Si, furthermore, renders even a smoother interface than the original surface.

Fig. 4 shows the gate voltage shifts of thermal polyoxide and N_2O-plasma polyoxide under positive and negative constant current stress of $1mA/cm^2$ and $10mA/cm^2$, respectively. N_2O-plasma polyoxide exhibits much smaller voltage shifts for both polarity stress in spite of 10 times larger stressing current. In addition, N_2O-plasma polyoxide shows significantly lower gate voltage shift when electrons are injected from the floating gate electrode.

To study the long term reliability of polyoxide, cumulative charge-to-breakdown(Qbd) characteristics were investigated. Fig. 5 shows that N_2O-plasma polyoxide has Qbd up to $10C/cm^2$, which is 30 times larger than thermal polyoxide. Through simple one-step N_2O-plasma oxidation, high quality polyoxide comparable to optimized ONO interpoly dielectric can be obtained [4].

Fig. 6 shows the SIMS depth profiles of N_2O-plasma polyoxide. Nitrogen atoms are pile-up at the polyoxide/poly-Si interface and form a nitrogen-rich layer. The chemical bonding structure of incorporated nitrogen atoms are studied by XPS analysis. The binding energy of 397.8eV as shown in Fig. 7 means that there exist strong Si-N bonds which has much stronger endurance under electrical stressing than Si-O bonds. Therefore, the lower trapping rate and larger Qbd is mainly attributed to not only the nitrogen-rich layer but also the smooth interface.

4. Conclusions

A simple growing technique of interpoly oxide using ECR N_2O-plasma has been investigated. N_2O-plasma polyoxide has a low leakage current and large Qbd, which leads to good data retention and high endurance properties when used as interpoly oxide of flash memories. Combination of in-situ doped a-Si with N_2O-plasma oxide is a good candidate for interpoly dielectric structure of future high density nonvolatile memories.

We will present the retention and endurance characteristics of NVMs at SSDM'97.

References

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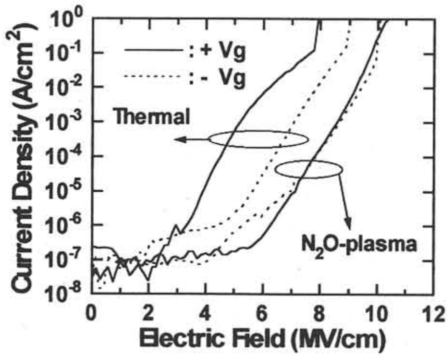

Fig. 1 Current density versus electric filed plots for thermal oxide and N_2O-plasma oxide on poly-Si (deposited in *in-situ* doping followed by thermal annealing for crystallization).

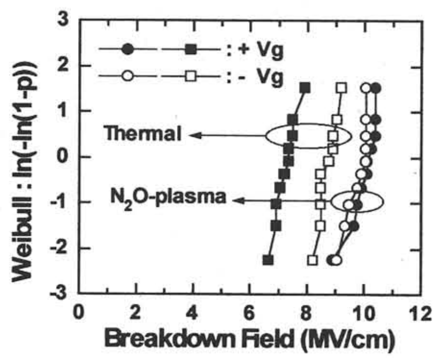

Fig. 2 Cumulative weibull distribution of breakdown field for thermal polyoxide and N_2O-plasma polyoxide

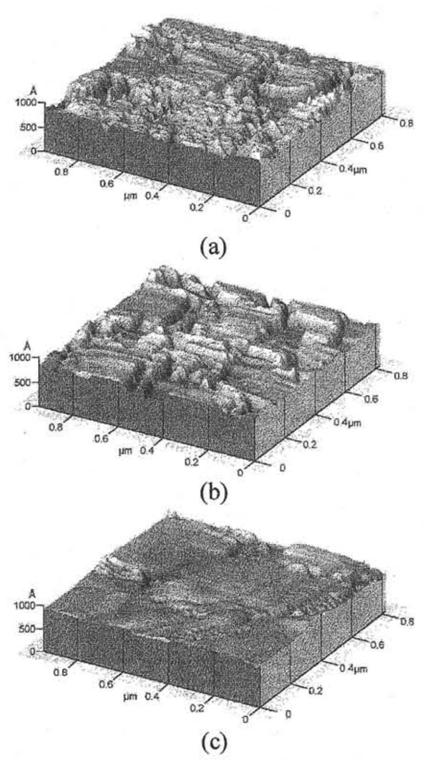

Fig. 3 AFM images of surface of poly-Si (a) without oxidation, (b) after thermal oxidation, and (c) after N_2O-plasma oxidation. The corresponding rms roughness are 6.4nm, 9.6nm, and 4.6nm respectively.

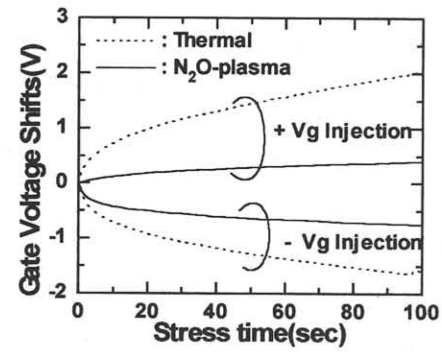

Fig. 4 Gate voltage shifts during constant current stressing with 1mA/cm^2 for thermal polyoxide and 10mA/cm^2 for N_2O-plasma polyoxide.

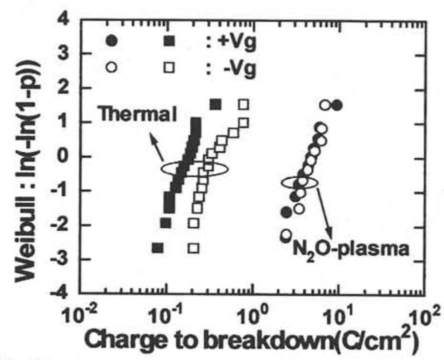

Fig. 5 Weibull plots of charge-to-breakdown of capacitors with thermal polyoxide and N_2O-plasma polyoxide, measured at current density of 10mA/cm^2.

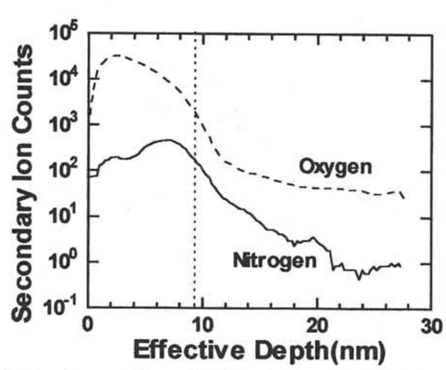

Fig. 6 SIMS depth profiles of N_2O-plasma polyoxide. The vertical dotted line indicates Si/SiO_2 interface.

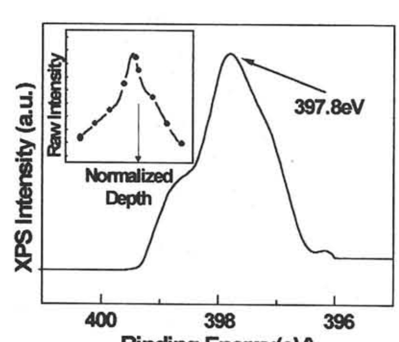

Fig. 7 XPS N(1s) intensity of N_2O-plasma oxide at the interface. Inset : depth profile of N(1s) intensity.