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Scaling of Flash Memory Interpoly Dielectrics Using NH_3-Annealed CVD SiO_2 Single-Layer Films

T. Kobayashi, A. Katayama, H. Kume and K. Kimura

Central Research Laboratory, Hitachi Ltd.,1-280, Higashi-koigakubo, Kokubunji, Tokyo 185, JAPAN
Phone: +81-423-23-1111, Fax: +81-423-27-7753, E-mail: takobaya@crl.hitachi.co.jp

1. Introduction

In flash memories, $SiO_2/Si_3N_4/SiO_2$ composite (ONO) films are used as interpoly dielectrics and their thicknesses have been reduced as device integration has advanced (Fig. 1). However, the reported thinning limit of the ONO is about 13 nm [1], which prevents reduction of the programming voltage. To overcome this problem, we have studied the use of CVD SiO_2 single-layer films as an interpoly because their physical thickness can be made much thinner [2]. In this paper, we discuss how the leakage current in these films can be reduced, which is a critical issue affecting the application of the CVD SiO_2, and the scalability of the films that are less that 10 nm thick.

2. Thinning Effect of the Interpoly Dielectrics

We first calculated the relationship between the tunnel-oxide thickness and the interpoly thickness under the condition that the injection is completed within 1 ms using a 0.25 μm-AND type memory cell [3] (Fig. 2). By thinning the interpoly, the device performances can be maintained when the tunnel-oxide thickness is increased to improve the tunnel-oxide reliability which is degraded by programming/erasing operations. The programming voltage can also be reduced by thinning the interpoly when the tunnel-oxide thickness is constant (Fig. 3).

However, to maintain the injection time and V_{th} shift, the electric field across the interpoly increases as the thickness is decreased (Fig. 4), and this increases the leakage current. Therefore, to allow further thinning of the interpoly, we must find a way to control the leakage current.

3. Interpoly Formation and Measurements

The process flow for NH_3-annealed CVD SiO_2 films is shown in Fig. 5. We measured the leakage current and trapped charge in the films by using two types of MOS capacitors: one with patterned edges of lower poly-Si as a floating gate (with edge), the other without the patterned edge (without edge) [2].

4. Leakage Current of the Interpoly

Next we tried to reduce the leakage current of the CVD SiO_2 films. We considered the cause of the leakage must be the defects (e.g. E' centers) in the films [4], and thought we could reduce their number by terminating nitrogen atoms through NH_3 annealing. Fig. 6 shows the J-E characteristics of the films when a positive bias is applied to the upper poly-Si. The leakage is reduced by more than two orders of magnitude by the NH_3 annealing. We found that this change in the leakage was determined by the nitrogen concentration in the films after annealing (Fig. 7).

The leakage current can be further reduced by thinning the films. Fig. 8 shows the F-N plots of NH_3-annealed CVD SiO_2 films with various thicknesses. The leakage for the capacitor with edges is dramatically reduced as the thickness is decreased. This leakage reduction results from the localized electric field at the pattern edges of the lower poly-Si. Fig. 9 shows the dependence of the electric field enhancement on the interpoly thickness, where the enhancement was obtained from the slopes of the F-N plots in Fig. 8 using a two-region model [2]. The localized electric field is reduced by the interpoly thinning because the electric field at the pattern edges increases with the ratio t_{ox}/r (t_{ox}: interpoly thickness, r: curvature radius of the pattern edge) [6].

The electric field across the interpoly increases as the film is thinned (Fig. 4), but this does not have to increase the leakage current, as shown in Fig. 10. This leakage decrease expands the operation margin and prevents interpoly degradation.

The interpoly thinning also makes it possible to reduce the programming voltage. Fig. 11 shows the relationship between the applied voltage to the control gates, V_{cg}, and the interpoly thickness under the condition of 1-ms injection. By reducing the interpoly thickness from 15.9 nm to 8.9 nm, V_{cg} is reduced by 2.8 V. This voltage reduction will be useful for peripheral MOS scaling.

5. Charge Trapping and Retention Capability

The thinning of the CVD SiO_2 films plays an important role in improving retention capability, where retention degradation is caused by charge trapping in the interpoly and the loss of charge. Fig. 12 shows the calculated V_{th} shift of the memory cells due to charge trapping in the interpoly. Trapped charges are easily detrapped from the interpoly, which degrades the retention capability. ΔV_{th} is obtained from the gate voltage variances when a constant current stress is applied to the films [7]. Because of the charge traps, ΔV_{th} increases with programming/erasing cycles in the case of a thicker interpoly, which results in retention degradation. In contrast, the ΔV_{th} is effectively controlled by thinning the films.

Charge loss caused by the leakage of the interpoly can also be controlled. By extrapolating the F-N plots of Fig. 8, we can see that the leakage is below the level necessary to avoid charge loss from the floating gates to the control gates through the interpoly when the film thickness is 8.9 nm.

6. Conclusion

NH_3-annealed CVD SiO_2 single-layer films are promising candidates for use as interpoly dielectrics of high-density flash memories. These films offer improved scalability compared to ONO films.

References

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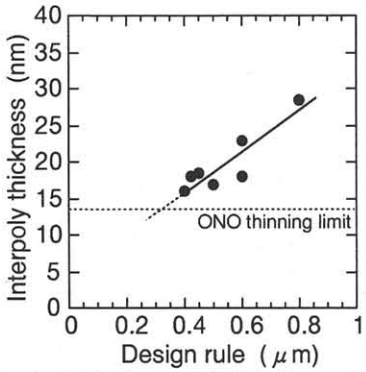

Fig. 1 Thinning trend of the interpoly dielectrics

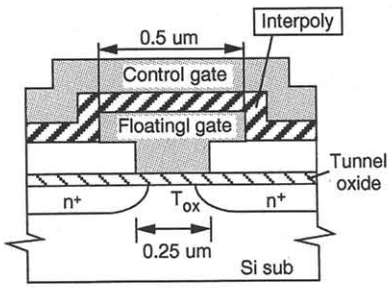

Fig. 2 Schematic diagram of 0.25- μ m AND type memory cell

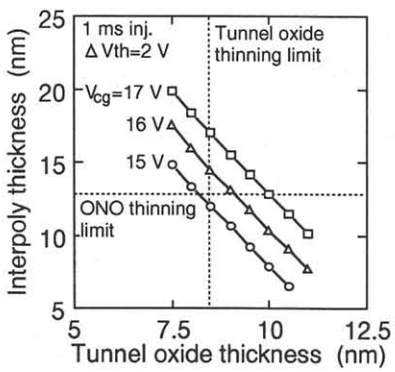

Fig. 3 Interpoly dielectric film thickness vs tunnel oxide thickness

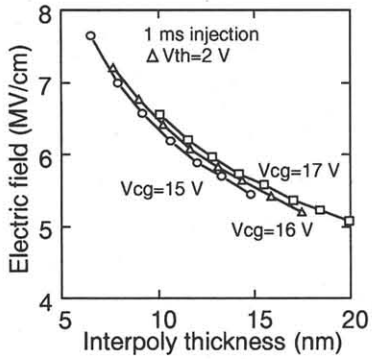

Fig. 4 Electric field across interpoly dielectric films after 1 ms injection

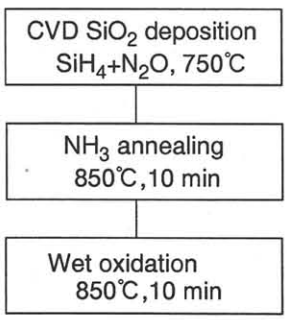

Fig. 5 Process flow for NH_3-annealed CVD SiO_2 single-layer interpoly

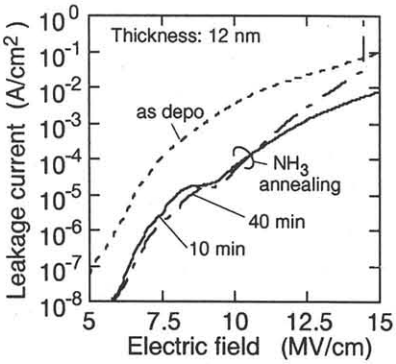

Fig. 6 J-E characteristics of NH_3-annealed CVD SiO_2 single-layer films

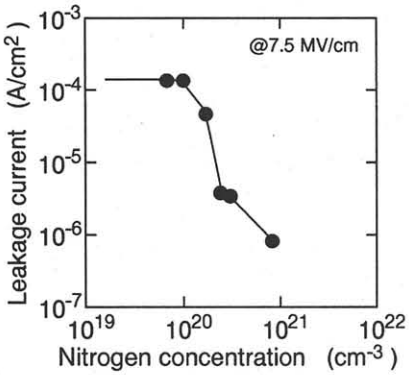

Fig. 7 Leakage current dependence on nitrogen concentration in the SiO_2 films

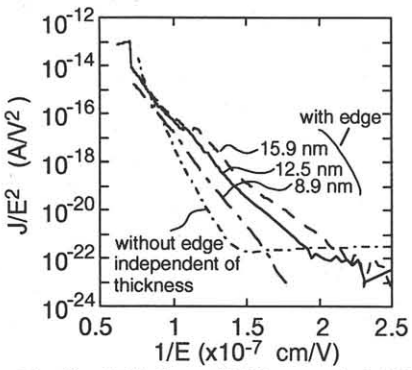

Fig. 8 F-N plots of NH_3-annealed CVD SiO_2 single-layer films

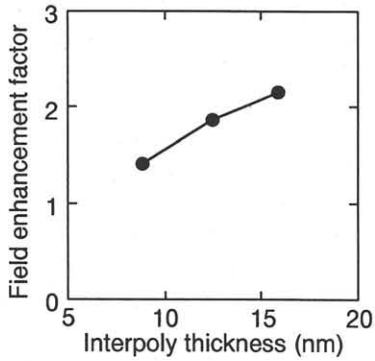

Fig. 9 Dependence of electric field enhancement on the interpoly thickness

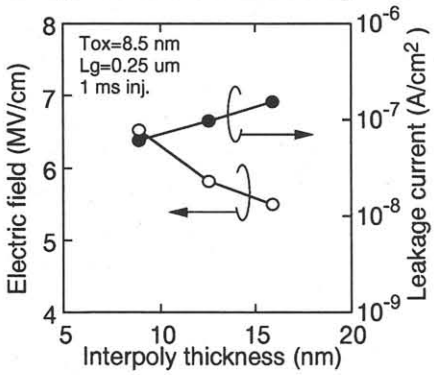

Fig. 10 Electric field and leakage current dependence on the interpoly thickness

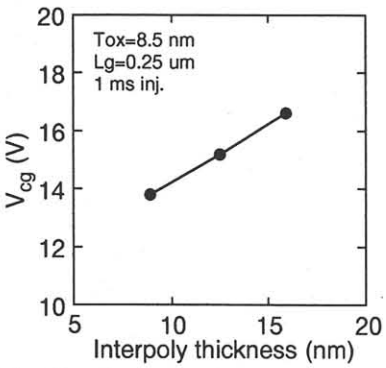

Fig. 11 Programming voltage reduction by thinning the interpoly thickness

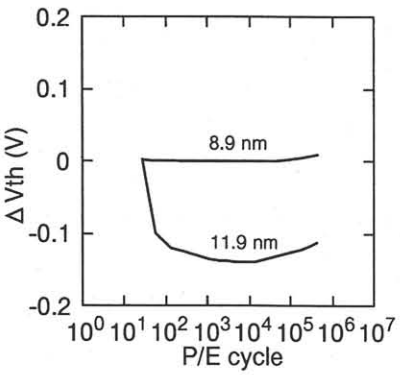

Fig. 12 Calculated V_{th} shift of the memory cell caused by charge trapping in the interpoly