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Invited

Reliability Concern of Ultra-Thin Gate Oxides

Akira Toriumi and Hideki Satake
Advanced Semiconductor Devices Research Laboratories, Toshiba Corporation
Isogo, Yokohama 235, Japan
Phone/Fax: +81-45-770-3688 / +81-45-770-3578, E-mail: toriumi@amc.toshiba.co.jp

1. Introduction

The strong push of SiO_2 research is partly related to the current Flash memory activity. On the other hand, the logic devices require even thinner oxides, where even the direct tunneling regime is considered. In this work, we discuss the comparison between thin and ultra-thin oxides in terms of the carrier transport and the dielectric breakdown, and the stress-induced leakage current.

2. Difference between thin and ultra-thin oxides except the thickness ?

(1) Carrier Transport

The conventional device physics has been described by the deterministic equation of electric field, but this will not be enough in very small size region such as the energy relaxation length. The oxide thickness is the smallest among device parameters, and even in the carrier transport in the amorphous SiO_2, it is comparable with the length for electrons to be energetically stabilized [1]. Therefore, below 10 nm the reliability should be examined by including the electron energy consideration.

The carrier transport in SiO_2 was studied by using the carrier separation experiment [2] both in n- and p-channel MOSFETs with 3.4 nm, 4.2 nm and thicker oxides. Oxides were thermally grown in the dry O_2 ambient. It has been found that the relationship between α = Isub/Ig in n-MOSFET and γ = Isd/Ig in p-MOSFETs in relatively thick oxides are well correlated [3]. However, in 3.4 nm oxide the hole generation mechanism looks different as shown in Fig. 1, which shows carefully measured Ig and Isub as a function of Vg for 3.4 nm and 4.2 nm oxide n-MOSFETs. Figs. 2 (a) and (b) show α and γ as a function of Vg. Fig. 2 (b) demonstrates that the injected electrons transport ballistically in SiO_2 in this thickness regime. On the other hand, note in Fig. 2 (a) that there are two types of direct tunneling both from the conduction band and from the valence band [4,5]. Direct tunneling electrons from the conduction band do not have enough energy to create holes in the gate electrode, but those from the valence band leave 100% holes in the substrate. Namely, there is a boundary of hole injection model into SiO_2 for thin and ultra-thin oxides, and the substrate hole accumulation method (Q_p) [6] is no longer valid in the ultra-thin oxide regime.

(2) Dielectric Breakdown

We investigated the TDDB characteristics both in thin and ultra-thin oxides. In this work, we obtained the TDDB results at a constant voltage stress. Fig. 3 shows $1/\tau_{bd}$ as function of applied gate bias. Note that the slope of the stress voltage dependence of $1/\tau_{bd}$ looks different between two oxide thickness. These results may imply that the limiting factor to the dielectric breakdown is gradually moving from the electric field to the electron energy, though the effect is not so significant in the present condition. In general, both effects work together, depending on the thickness and the bias condition. It suggests that we have to carefully consider the acceleration test of the reliability in thinner oxide region. The injection polarity effect of TDDB is another controversial issue. It will be shown that it is not an artificial but a real effect. The results might be due to the poorer structural relaxation in thinner oxides [7,8]. Though the oxides used in this experiment was not optimized for ultra-thin regime, we think that the results will be quite general. More attention should be paid to the Si/SiO_2 interface quality, which goes without saying that it is the most fundamental of MOS device technology.

(3) Stress-induced Leakage Current (SILC)

The SILC is also related to defects created by energetic electrons [9]. Fig. 4 shows the SILC as a function of the stressing voltage. It is found that there exists a clear threshold energy to observe the SILC even in the 4.2 nm oxide. In the thinner oxides, the direct tunneling leakage current becomes dominant and the SILC will be no more observed.

3. Summary

The ultra-thin oxides have been recently often discussed from the viewpoint of the device performance such as gm, Vth, or other short channel effects. In this paper, some differences between thin and ultra-thin oxides are presented from the experimental results of the carrier transport, the dielectric breakdown and the stress-induced leakage current. Concerning the SILC, there might be a very small thickness window between the SILC immune region and the direct tunneling region. In the dielectric breakdown, both defect creation and structural deformation occur simultaneously with different stress condition dependence. This fact makes understanding of the breakdown complicated. Practically, the acceleration test

should be reconsidered in this oxide thickness regime.

Acknowledgment

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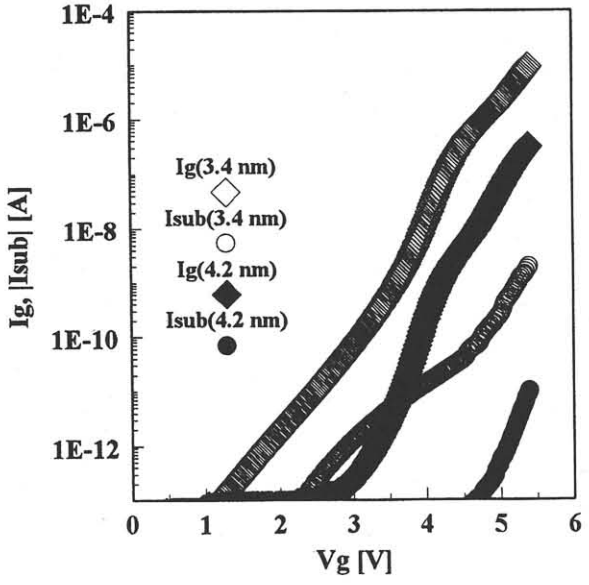

Fig. 1 Ig and Isub as a function of Vg for 3.4 nm and 4.2 nm oxide n-MOSFETs.

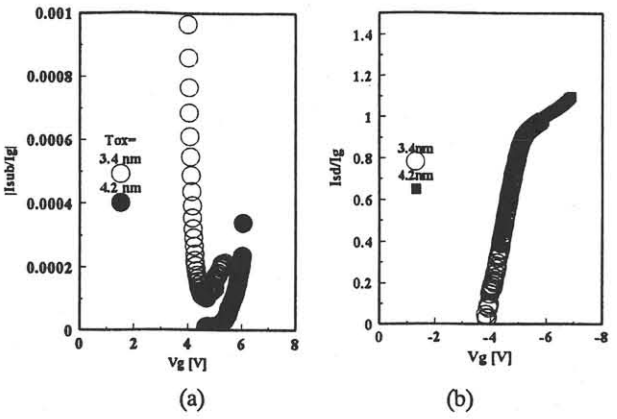

Fig. 2 Substrate hole generation efficiency, α, (a) measured in n-MOSFETs and quantum yield for impact-ionization, γ, (b) in Si as a function of Vg measured in p-MOSFETs.

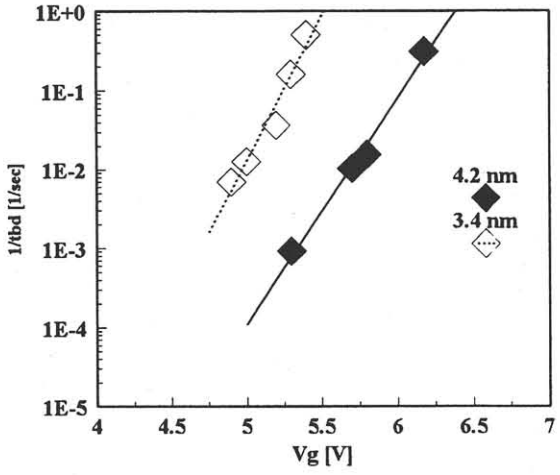

Fig. 3 $1/\tau_{bd}$ as a function of applied gate bias for 3.4 nm and 4.2 nm oxide n-MOSFETs

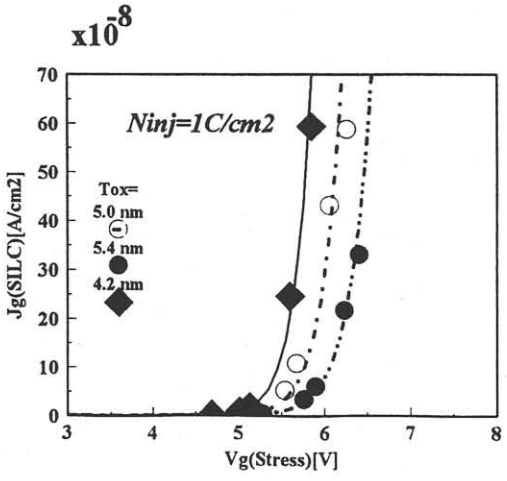

Fig. 4 Stressing voltage dependence of stress-induced leakage current measured in various oxide thickness n-MOSFETs