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An Experimental Evidence to Link the Origins of "A Mode" and "B Mode" Stress Induced Leakage Current

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1. Introduction

Advance of Si MOS LSIs will not be possible without highly reliable ultrathin gate oxides[1]. Therefore, it is strongly required to reveal the breakdown mechanism in the ultrathin silicon dioxides. We proposed that the breakdown mechanism consists of following two processes[2]; the partial breakdown (p-BD) and the complete breakdown (c-BD). The p-BD is also called "quasi-breakdown"[3] or "soft-breakdown"[4]. Although we discussed the breakdown mechanism after the occurrence of the p-BD[5], the mechanism to induce the p-BD has not been clarified.

It is well known that two modes of stress induced leakage current (SILC) can be observed in ultrathin oxides, the "A mode" (A-SILC)[6] followed by the "B mode" (B-SILC)[7]. The B-SILC is induced by the p-BD at a local spot and, hence, the degradation mechanism of both SILCs is expected to give invaluable information to reveal the partial-breakdown mechanism. In this paper, the concept of "threshold A-SILC" to induce the p-BD is introduced for the first time, and it is shown that both SILCs have a same origin but different conduction mechanisms.

2. Experimental

3.8 ~ 4.3 nm–thick oxide films were grown on CZ-p type Si (100) substrates using various fabrication processes. Electrical characteristics were measured using MOS capacitors with n^+ polycrystalline silicon gate electrodes.

3. Results and Discussion

Threshold A-SILC to Induce the B-SILC

By performing the electrical stressing to the ultrathin oxides, the A-SILC monotonously increases and, in contrast, the B-SILC appears abruptly[7] as shown in Fig. 1.

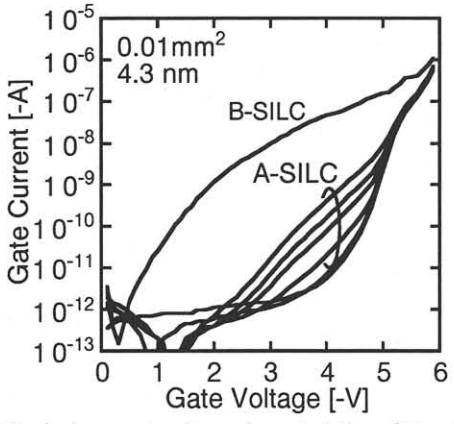

Fig. 1 Typical current-voltage characteristics of two SILCs.

To clarify the relationship between A-SILC and B-SILC, oxide films were performed constant-voltage stressing until the occurrence of p-BD with monitoring the current level of A-SILC. The A-SILC as a function of stressing time is plotted in Fig. 2 for (a) sample A under various stressing fields, and (b) samples B, C and D having various oxide integrity. The occurrence of the p-BD is also shown with triangular marks(∇). It is clear that the p-BD occurs when the A-SILC becomes a threshold value, 1~3 μA/cm² in this case, and the threshold value does not depend on the stressing field or the oxide integrity. In contrast, the threshold A-SILC decreases with increasing the gate area as shown in Fig. 3. This indicates that the p-BD occurs at a spot where a condition to induce the p-BD is locally satisfied by chance. This model is supported also by the gate area dependence of the time to partial-breakdown[8].

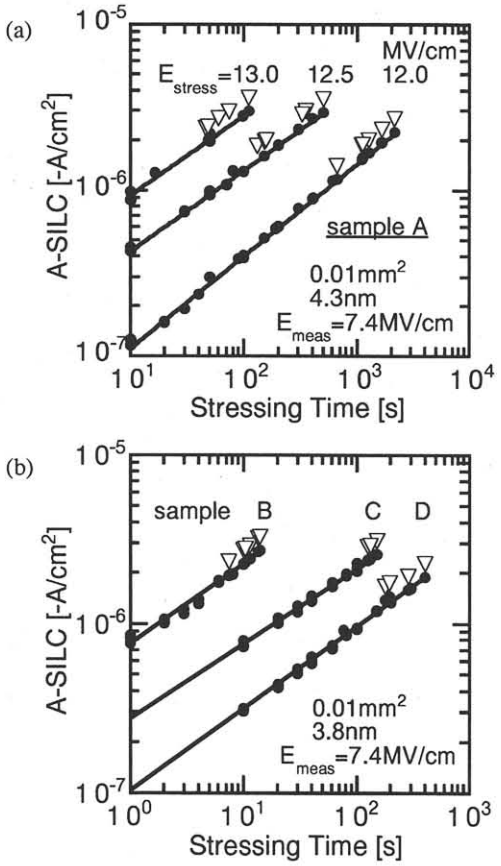

Fig. 2 The A-SILC at the gate voltage of -4V as a function of stressing time for (a) various electric fields, and (b) three samples having various oxide integrity. Triangular marks (∇) show the occurrence of the partial-breakdown.

Consistent Model to Link the Origins of Both SILCs

Above results suggest that both SILCs have a same origin but different conduction mechanisms. To confirm this, an abrupt current increase from A-SILC to B-SILC must be explained consistently. Although Depas *et al.*[4] proposed a qualitative model to link both SILCs, they explained with the same conduction mechanism, trap assisted tunneling (TAT), for both SILCs and, therefore, their model fails to explain the above problem and the different characteristics of both SILCs[7]. In fact, only B-SILC depends on the temperature as shown in Fig. 4. Although the B-SILC is constant at a given voltage without depending on the oxide integrity or stressing condition[2], it is rarely observed that B-SILC saturates after experiencing small levels. In Fig. 4, the gate current is plotted for capacitors having various levels of B-SILC and A-SILC.

As the conduction mechanism of the B-SILC, we proposed[9] the variable range hopping (VRH) conduction [10], which is mediated by the hopping sites, i.e., the defect sites including various trap sites and the interface states. The current, I_{VRH}, is expressed as follows[10];

$$I_{VRH}(T) = \alpha \cdot \exp(-\beta \cdot T^{-1/4}) , \quad (1)$$

$$\beta = 2.06 \, (f_D \cdot k_B)^{-1/4} , \quad (2)$$

$$f_D = \gamma^3 \cdot N , \quad (3)$$

where T is the temperature, k_B is the Boltzmann's constant, f_D is the defect density factor, γ and N is the decay length and the density of the hopping sites available for carrier conduction, respectively. At lower temperature range, in contrast, no temperature dependence is observed and the trap assisted tunneling current via hopping sites, I_{TAT}, is considered to be dominant[10]. It is well known as the "Anderson transition" that the VRH current abruptly appears when the density of hopping sites reaches to a threshold value[10]. Hence, it is easily explained that gradual increase of f_D results in an abrupt increase of the current from A-SILC to B-SILC by considering that A-SILC corresponds to I_{TAT}.

In Fig. 5, I_{VRH} and I_{TAT} obtained as B-SILC at 300 K and 80 K, respectively, are plotted as functions of f_D calculated from Fig. 4. Once the p-BD occurs, the gate current abruptly increases by more than a few orders from $I_{TAT}(f_D)$ to $I_{VRH}(f_D)$ even if f_D is quite uniform in the entire oxide area. Note that f_D at the spot where p-BD occurs is larger than that of averaged over whole oxide area.

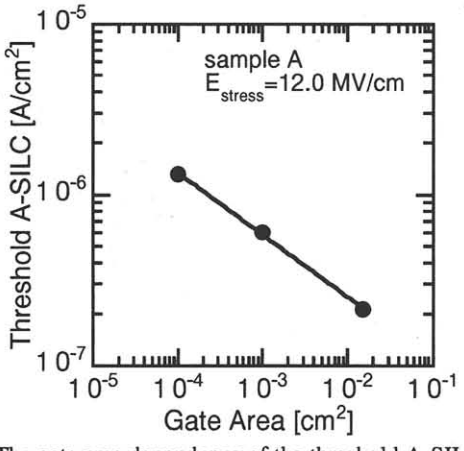

Fig. 3 The gate area dependence of the threshold A-SILC.

4. Conclusion

The concept of the "threshold A-SILC" to induce the p-BD is introduced for the first time. It is also shown that A-SILC and B-SILC have a same origin and that the abrupt current increase and different temperature dependence before and after the p-BD can be consistently explained by the gradual increase of the defect sites generated by stressing.

Acknowledgment

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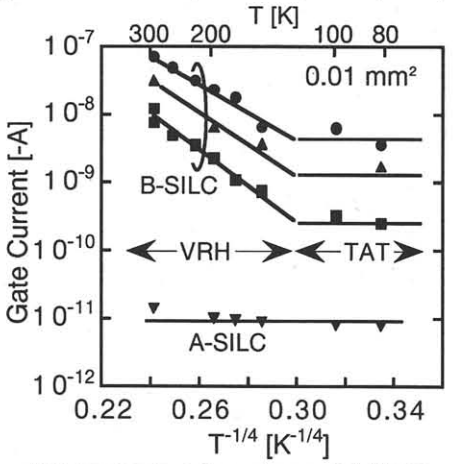

Fig.4 The temperature dependence of A-SILC and B-SILC.

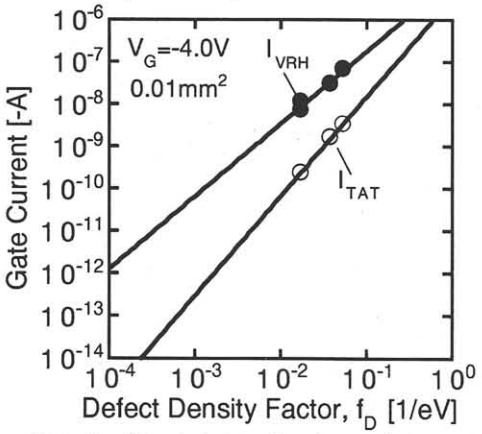

Fig.5 Relationships between I_{VRH}, I_{TAT} and the defect density factor (f_D). I_{VRH} and I_{TAT} were obtained from the B-SILC at 300K and 80K, respectively, shown in Fig. 4.