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Drain Disturb Relaxation by Substrate bias Selecting Scheme for Sector Erase Flash Memory with Conventional Single Stacked Gate Cell Structure

M.Yoshimi, N.Shinmura, T.Tanigami, K.Hakozaki , S.Sato, and K.Iguchi

VLSI Development Laboratories, IC Tenri Group, SHARP Corporation
2613-1, Ichinomoto, Tenri, Nara, 632, Japan
PHONE: (07436) 5-4037, FACSIMILE: (07436) 5-2774

1.Introduction

Recently high density flash memory has been expected to replace the external mass storage device market of computers. For this application, fast random access, low power consumption, and small erase unit size are required. To realize a small erase unit, it is necessary to improve the disturb characteristics. Several cell structures has been proposed for low power supply sector erase flash memory using FN program. However, these cells require additional process steps for select transistors and the new process technology for local bit line fabrication [1-5]. In addition, access time of these cells are longer than that of the conventional single stacked gate cell. In this paper, we proposed a new drain disturb relaxation technology by substrate bias selecting scheme for FN programming single stacked gate cell that can be fabricated in conventional process flow.

2.Memory cell and array architecture

A conventional single stacked gate structure was adopted in this study. 0.35μm 2-layer poly, 2-layer metal triple well CMOS technology was applied to fabricate this structure. The tunnel oxide thickness is 10nm, ONO effective thickness is 16nm. As shown in Fig.1, each 64kbyte block is divided up 32 sectors, which electrically corresponds to 1K bytes/sector. And an array in a sector is composed of 512 bit lines and 16 word lines. The p-well of each sector is surrounded by deep n-well so that each one can be selected.

3.The program/erase characteristics

The memory cell is erased by tunnel injection from the whole channel region. In a program operation, electrons are ejected from the floating gate to the drain. Fig.2 shows the typical program and erase characteristics of a single memory cell. The cell Vth can be increased to more than 3.3V in 200μsec, which is 10% higher than the control gate voltage at read operation. And the cell Vth can be decreased to less than 1.5V in 100μsec. Considering a wide Vth distribution of FN programming, we assumed the longest program time is 1msec, which is one decade longer than that of a typical cell. Substrate disturb during erasure is eliminated by the separating p-well and source line for each sector. The operating bias conditions are summarized in Table.1.

4.Drain disturb relaxation technology

Drain disturb is an undesired programming of an unselected cell during programming of other cells on the same bit line. In sector erase, drain disturb is magnified by program/erase cycles, because a certain sector is affected by program/erase cycles of all other sectors in a same block. The maximum drain disturb time for the unselected cell is 1E5 sec, which is calculated as 1msec (program time) x 16 word lines x 64 sectors x 1E5 Program /erase cycles.

The reduction of the electric field between the floating gate and the drain is necessary to suppress the drain disturb, but there was no adequate method other than local bit line scheme with select transistors. As one of the alternative method, we studied a new scheme that the positive voltage is applied to the control gate of the unselected sectors. But when the positive voltage is applied to the control gate, source-drain current flows because the low Vth cells easily turn on. To prevent this problem, substrate bias selecting scheme is proposed.

The Vth of the memory cell can be increased by back gate effect without changing the floating gate charge as shown in Fig.3. Therefore, Vcg as high as ΔVth can be applied to the control gate without increasing the source-drain current. In addition, since the subthreshold swing S is reduced when the back gate bias is applied, the higher Vcg than ΔVth can be be applied to the control gate.

To clarify whole effect of the substrate bias, the source-drain current of a cell was measured as a function of the substrate bias. The result is shown in Fig.4. The source-drain current when Vcg=2V,Vsub=-2V was suppressed to the same as that when Vcg=Vsub=0V.

In this case, the decrease of the voltage between the floating gate and drain is calculated as follows.

$$\Delta Vfg=GCR \cdot Vcg+CCR \cdot Vsub=0.8V$$

where GCR is the gate coupling ratio(0.6), CCR is the channel coupling ratio(0.2); Vcg is the control gate voltage(2V); Vsub is the back gate bias(-2V)

As shown Fig.5, the life time when Vd=5V with substrate bias scheme is nearly same as the life time when Vd=4.2V without substrate bias scheme. The drain disturb life time was magnified by 2 decades by substrate bias selecting scheme. This result gave relatively good agreement with improvement estimated by above simple calculation.

As a result, the drain disturb life time which is sufficient for small sector erase can be achieved without select transistors and local bit line by using this technology.

5.Summary

A new drain disturb relaxation technology by substrate bias selecting scheme is proposed. By using this method, the drain disturb life time is drastically improved. This life time has sufficient margin for small sector erase operation without sector select transistors and local bit line structure. This technology enables low cost, high speed, high-density, low power supply sector erase flash memory.

Reference
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[2] H.Kume et. al. IEDM Tech. Dig., pp.991, 1992
[3] Y.S.Hisamune et. al. IEDM Tech. Dig., pp.19, 1993
[4] M.Kato et. al. IEDM Tech. Dig., pp.921, 1994
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Table.1 Operating bias conditions

Mode	Sector	Cell	WL	BL	SL	p-well
Program	Select	Select	-11V	5V	open	0V
		Unselect	0V	0V	open	0V
	Unselect		+2V	+5V	open	-2V
Erase	Select		9V	open	-9V	-9V
	Unselect		0V	open	0V	0V
Read	Select	Select	3V	1V	0V	0V
		Unselect	0V	0V	0V	0V
	Unselect		0V	0V	0V	0V

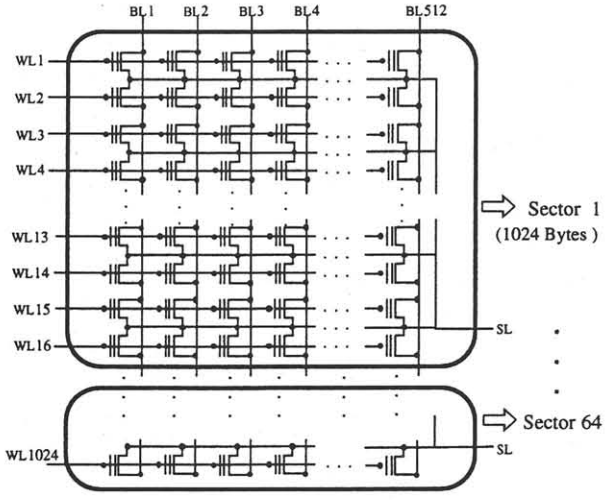

Fig.1 Memory Cell Array Architecture

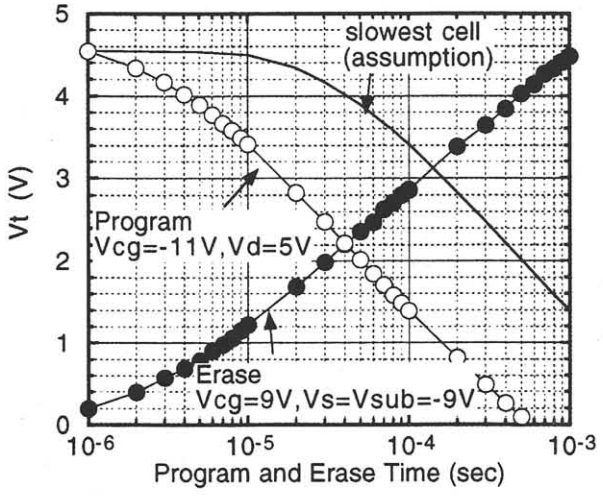

Fig.2 Program and Erase Characteristics

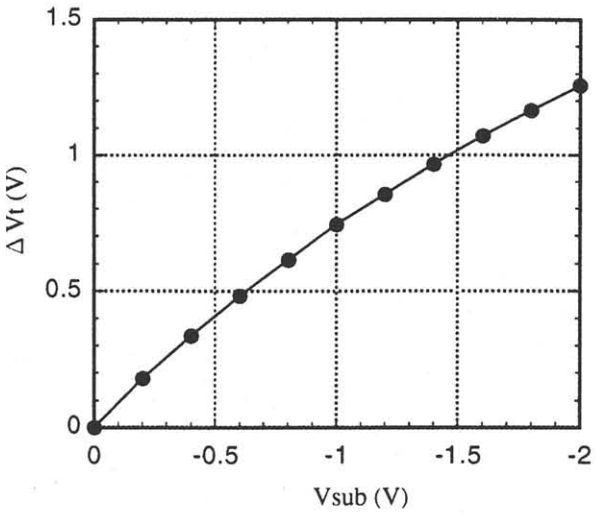

Fig.3 Memory cell Δ Vth dependence of Substrate bias (Back gate effect)

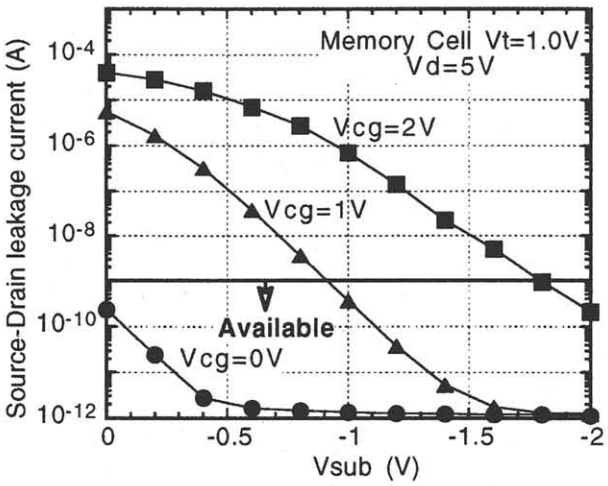

Fig.4 Source-Drain leakage current dependence of Substrate bias

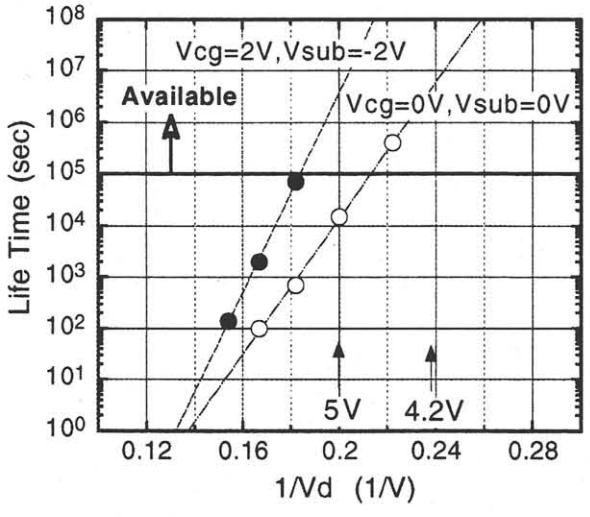

Fig.5 Drain disturb characteristics