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Byte Erasable NOR Flash EEPROM with Double Diffused Drain for High Programming Speed

M.K. Cho, K.H. Yum, K.S. Kim, J.H. Choi, S.T. Ahn, and Dae M. Kim*
Memory Division, Semiconductor Business, Samsung Electronics Co., LTD.
San #24, Nongseo-Lee, Kiheung-Eup, Yongin-City, Kyungki-Do, 449-900, Korea
*Department of Electrical Eng., Pohang University of Science and Technology, Kyungbuk, Korea

Introduction

The conventional stacked gate NOR flash cell uses an abrupt drain junction to enhance the hot electron generation for high speed programming and adopts a graded source junction for source side erase[1]. However, such an erasing scheme cannot avoid large erase sector size and thus limits the application of the flash memory to the systems.

In this paper, we demonstrate that a "reverse" cell structure with a graded drain junction and an abrupt source junction have many advantages over the conventional cell. With the drain side erasing scheme, byte erase is possible. The graded drain junction extends the hot electron injection area down to the mid-channel. This significantly improves the programming efficiency and reduces the power consumption.

Cell Structure

Fig. 1 shows the schematic and SEM cross section of the memory cell. The structure has a double diffused graded drain junction. The cells with a unit cell size of 1.8 μm^2 are fabricated using the 0.5 μm technology. The tunnel oxide and the effective interpoly ONO thicknesses are 9 nm and 15 nm, respectively.

Cell Operation

The cell operation conditions are summarized in Table 1. Hot electron injection and Fowler-Nordheim tunneling at the drain side are used for programming and erasing, respectively.

The graded drain junction increases the junction breakdown voltage and reduces the band-to-band tunneling leakage current. This enables the drain side erase operation. The drain side erase characteristics in Fig. 2 show acceptable erasing speed of about 10 ms. Fig. 3 shows the erase disturbance in unselected cells measured from a 512kb cell array with 512 word lines. After the erase stress for 5.11s (10 ms × 511 unselected cells), Vth shift of the "reverse" cell is negligible because of the large drain coupling ratio with a long gate/drain overlap. The graded junction under the floating gate significantly reduces the band-to-band tunneling current[2], as shown in Fig. 4. These results suggest that we can erase the cell in byte unit using drain side erase.

Programming characteristics of the reverse memory cell with double diffused drain are compared to those of the conventional cell. Fig. 5 shows the ratio of the gate current to the drain current. One notes that the reverse cell has the programming efficiency more than ten times higher than that of the conventional cell. One time programming characteristics shown in Fig. 6 suggests that the reverse cell consumes less current, about 50 % of the conventional case. Fig. 6 also shows the cell can be programmed at 2.3V with 1 kΩ bit line loading. As shown in Fig. 7, the programming speed of the reverse cell is faster than the conventional by nearly one order of magnitude. Furthermore, the cell can be programmed in 50 μs at Vd = 3V. This means that high density NOR flash memories with 3V single power supply can be achieved without the high voltage generation scheme.

It has been generally believed that the drain side must have an abrupt junction in order to enhance the hot electron generation rate and thus the program speed. However, results in this study show that the double diffused drain junction has superior programming characteristics. Device simulation results in Fig. 8 show that the peak lateral electric field of the reverse cell is lower than the conventional case. However, extension of the hot electron generation point to the mid channel and the presence of the vertical field in the n^- region increases the hot electron injection probability and thus the programming efficiency.

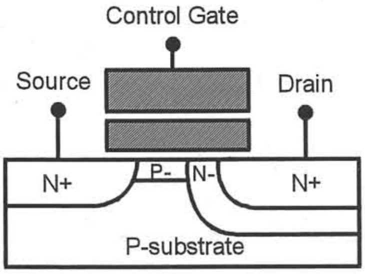
The read retention characteristics are sufficient, as shown in Fig. 9. Fig. 10 shows that this cell has satisfactory endurance characteristics of up to 10^5 program/erase cycles.

Conclusion

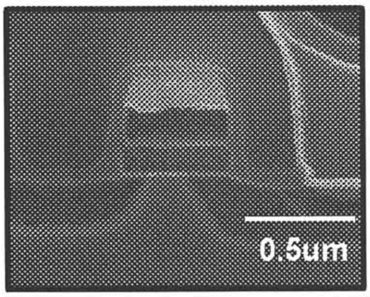
With the double diffused drain cell, it is possible to erase the device in byte unit and thus overcome limitation of the large erase sector size in flash memories. Compared to the conventional cell, this cell has faster programming speed and consumes less power. It is also possible to program the cells with a single 3 V power supply. The reliabilty characteristics of the cell are confirmed. The byte erasable cell with double diffused drain is a promising technology for broadening the use of flash memories.

References

[1] H.Kume et al., IEDM Tech. Dig., p.560 (1987).
[2] R.Shirota et al., IEDM Tech. Dig., p.26 (1988).



(a)



(b)

Fig.1 (a) Schematic and (b) SEM cross section of the memory cell with a double diffused drain junction.

Table 1. Operating conditions of the memory cell.

	Program	Erase	Read
Vd (V)	3.0~ 5.0	5	1.0
Vcg(V)	9.0~12.0	-10	3.0~5.0
Vs (V)	0	Floating	0
Vb (V)	0	0	0

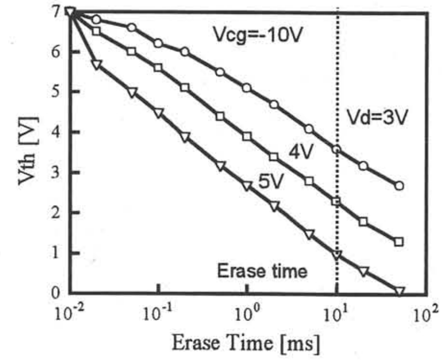


Fig.2 Characteristics of drain side erase.

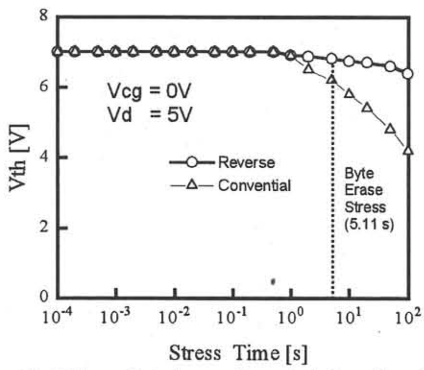


Fig.3 Erase disturbance characteristics of unsel-ected cells. "Reverse" cell represents the cell in Fig.1, while the conventional cell has an ab-rupt drain junction and a graded source junction.

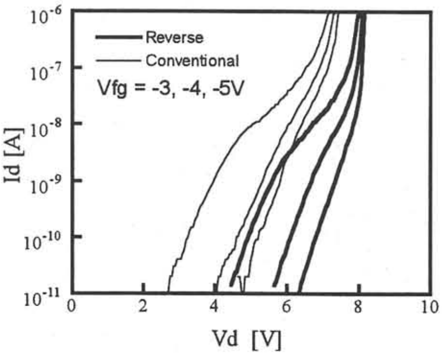


Fig.4 Band-to-band tunneling current of the reverse and conventional cells.

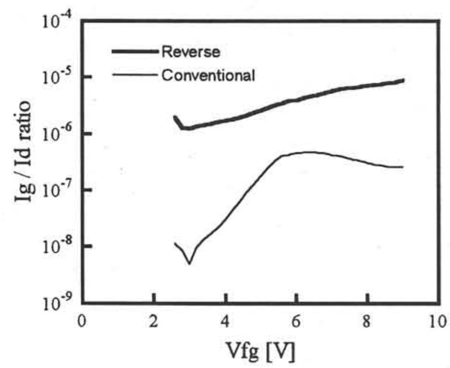


Fig.5 Ratio of the gate current to the drain current with respect to the floating gate voltage.

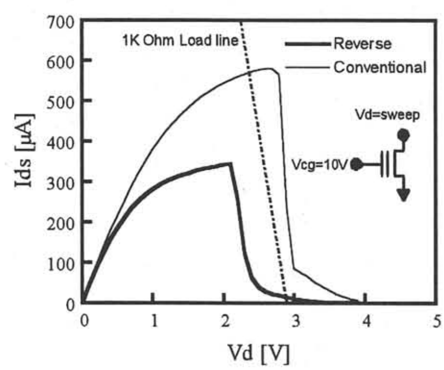


Fig.6 One time programming characteristics.

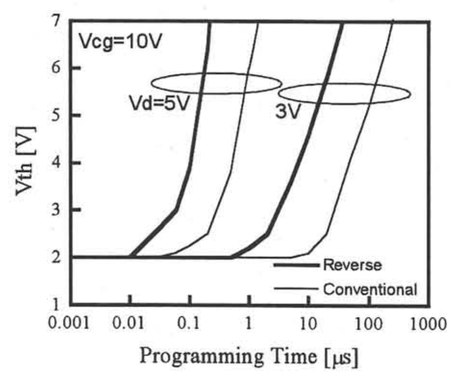


Fig.7 Programming characteristics of the reverse and the conventional cells.

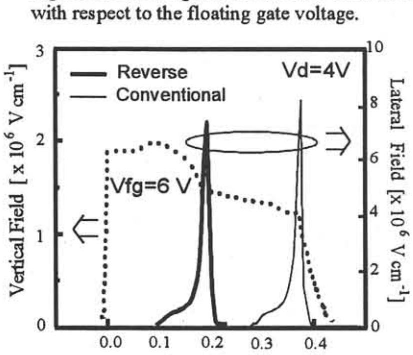


Fig.8 Two-dimensional MEDICI simulation result of the lateral and vertical electric field in programming condition. The effective cha-nnel length is 0.4 μm.

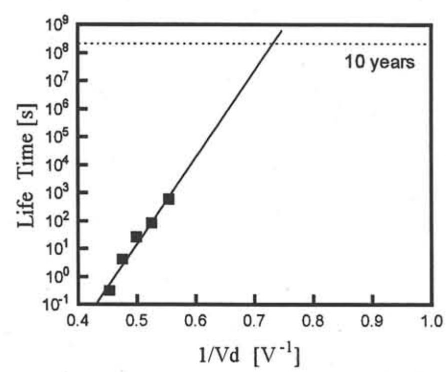


Fig.9 Read retention characteristics.

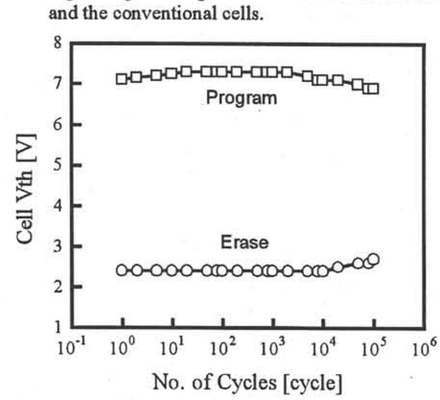


Fig.10 Endurance characteristics.