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# Suppression of Hole Injection into the Tunnel Oxides of Flash Memories

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## 1. Introduction

The reliability of the oxide greatly affects the storage reliability in Flash memory. Recently, it has been suggested that oxide degradation (stress-induced leakage current and dielectric breakdown) correlates with holes injected into the oxide during Fowler-Nordheim (F-N) tunnel injection of electrons[1,2]. Therefore, in this paper we investigate ways to reduce the hole injection with respect to several variables, especially the geometry of the gate edge, through a two-dimensional device simulation.

## 2. Simulation

We have constructed a new device simulator for Flash memories, which is based on CADDETH [3]. This simulator includes models for the F-N tunneling current [4], band-to-band tunneling (BTBT)[5], impact-ionization (II) induced by electrons injected into the anode [6], and hot-hole injection from the channel [7]. With this simulator, for the first time, it has become possible to separately evaluate the electron $I_e$ and the hole $I_h$ components in a gate current and their spatial distributions. Since a low $I_h$ is expected to bring about higher reliability in the Flash-memory oxide, we have investigated how to reduce $I_h$ with respect to the source voltage $V_S$, source/floating gate overlap length $X_S$, bird's beak length $X_{BB}$, and impurity profile in the source. Holes are assumed to be generated by the II of injected electrons in the anode and/or BTBT near the source depletion layer, then they are injected into the oxide. The device structure assumed in our simulation is shown in Fig.1. The gate width was 0.5μm, and the default bias conditions were source voltage $V_S$=4V, control gate voltage $V_{CG}$=-10V, and drain voltage $V_D$=floating. The default structure has no bird's beak (but a radius of curvature $r_c$ =10 nm) and $X_S$=100 nm.

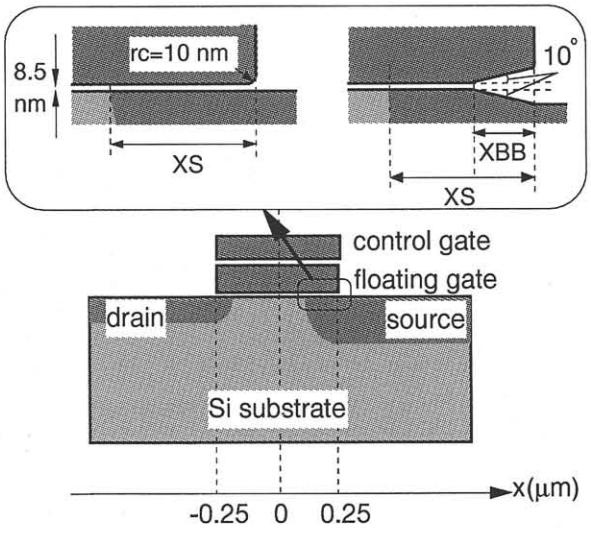


Fig. 1. Cross section of the device structure assumed in the device simulation and a definition of coordinate x.

## 3. Results and Discussion

First, we evaluated the gate current for $V_S$ ranging from 0 to 5V as a function of the voltage difference between the floating gate and the source. Figure 2 plots the $I_e$ and $I_h$ - voltage characteristics. $I_e$ is not dependent on $V_S$ as expected, but $I_h$ increases with $V_S$. The distribution of the hole current density along a substrate/oxide interface at the beginning of an erase operation is plotted in Fig. 3. The peaks at the gate-edges are due to the gate edges' sharpness. The distribution of holes due to II is similar to that of electrons and its magnitude is about two orders lower. Note that an additional peak appears near the junction (x~0.15 μm) which originates from BTBT, and that the peak value increases with $V_S$. Therefore, the dependence of $I_h$ on $V_S$ should be attributed to the BTBT [8]. A lower $V_S$ leads to a lower $I_h$, but requires a highly negative $V_{CG}$.

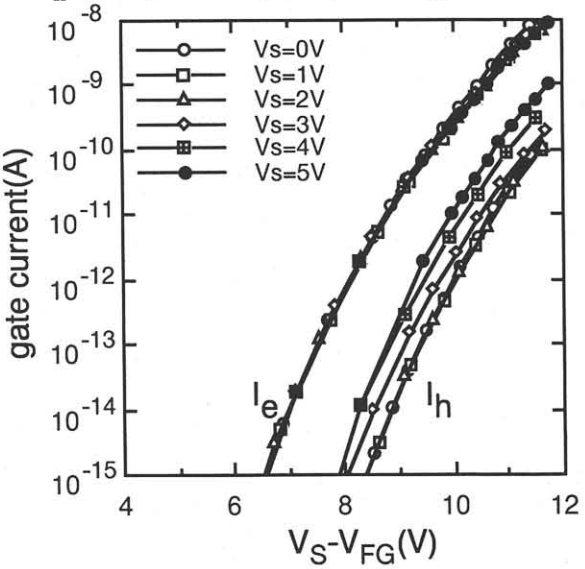


Fig. 2. Electron and hole components in the gate current versus the voltage difference between the source and floating gate.

Next, we looked for ways to suppress the BTBT under the default bias conditions. The BTBT depends on the electric field in a depletion layer; that is, the impurity profile in the source. First, we investigated the dependence of BTBT on $X_S$. In general, $I_e$ depends on both the oxide field, which is a decreasing function of $X_S$, and the area, which is an increasing function of $X_S$. We found the latter to be

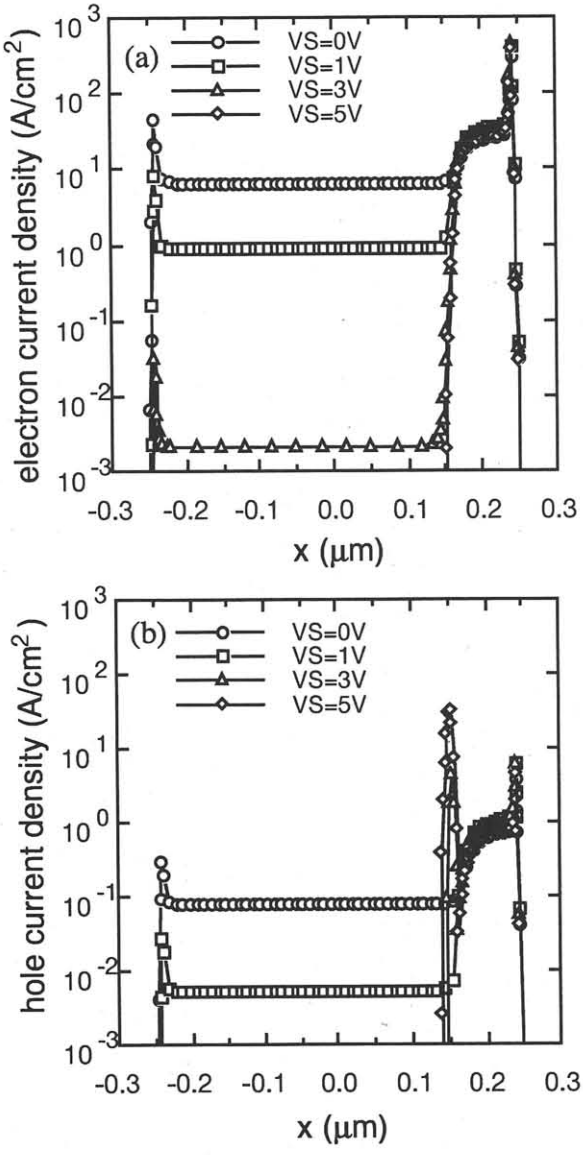


Fig. 3. Gate current density distribution along the substrate/ oxide interface: (a) electron component, (b) hole component.

dominant in our device structure. The hole density produced by BTBT, which is dominant in $I_h$, decreases as $X_S$ increases because the impurity profile in the source becomes smoother. We found that $I_e$ increased with $X_S$, but $I_h$ decreased.

On the other hand, as the implantation density becomes larger, $X_S$ increases. However, the peak of the hole current distribution shifts toward the drain region keeping the peak value nearly constant, since the electric field in a depleted region changes little. Therefore, the ratio of $I_h$ to the total gate current is nearly independent of the implantation density.

However, the source impurity profile dependence of $I_h$ is expected to be large. As an example, we examined a DDD (double diffused drain) structure that had a P-implanted layer as an $n^-$ layer and found that $I_e$ scarcely changed but $I_h$ decreased as the P-implantation density increased.

Finally, to investigate the effects of the gate-edge shape on

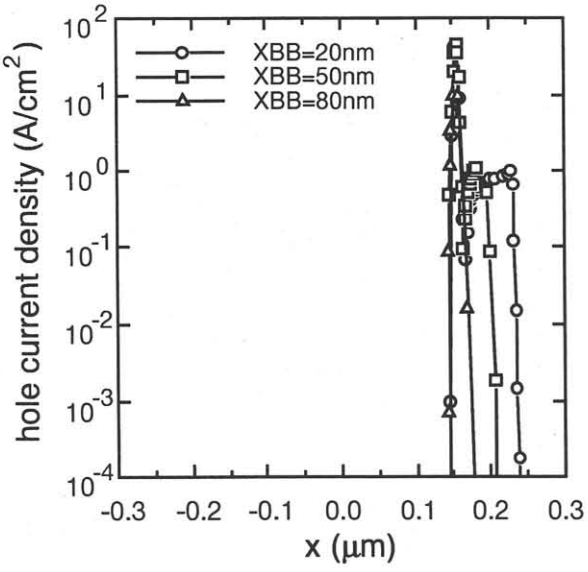


Fig. 4. Hole gate current density distribution along the substrate/oxide interface.

$I_h$, we evaluated $I_h$ in the presence of a bird's beak. Although $I_e$ is a decreasing function of $X_{BB}$, hole density produced by BTBT is so large that the dependence of $I_h$ on $X_{BB}$ is small unless $X_{BB}$ becomes larger than $X_S$. This can be explained in terms of the hole current distribution along the substrate/oxide interface plotted in Fig. 4. As $X_{BB}$ increases, the ratio of the hole component to the gate current increases. If $X_{BB}$ is larger than $X_S$, the gate current decreases significantly because the gate current flows through the oxide only above the channel. Therefore, it is desirable that $X_{BB}$ be small, even though an extremely small $X_{BB}$ leads to a concentration of current at the edge (Fig. 3), which may cause a rapid degradation of the oxide.

## 4. Conclusion

We have developed a new device simulator, which is able to evaluate the electron and hole components in a gate current, and applied it to the analysis of holes injected in an erase operation of a Flash memory. We found that this simulator enables us to optimize the cell structure and the write/erase scheme of a Flash memory to improve reliability.

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**References**

1) A.Teramoto *et al.*: *Proc. Int. Rel. Phys. Symp.1996* (1996)p.113.
2) H.Satake *et al.*: *Proc. Int. Rel. Phys. Symp.1997* (1997)p.156.
3) T.Toyabe *et al.*: IEEE Trans. Electron Dev. **32**(1985)p.2038.
4) J.Suñé *et al.*: IEEE Trans. Electron Dev. **39**(1993)p.1732.
5) A.Schenk: Solid-State Electron. **36**(1993)p.19.
6) K.F.Schuegraf and C.Hu: IEEE Trans. Electron Dev. **41**(1994) p.761.
7) C.Huang *et al.*: *Proc. Int. Rel. Phys. Symp.1995* (1995)p.61.
8) H.-J.Wann *et al.*: *Symp. on VLSI Tech.1993* (1993)p.81.