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Reduction of Junction Leakage Current Variation in MeV P Implant

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1.Introduction

MeV implantation is useful to form a retrograde well and a bipolar buried layer. However, anomalous increased leakage current was observed, when P ions were implanted at 0.7-3MeV with $1x10^{14}cm^{-2}$, followed by furnace annealing[1]. This reason was identified by cross-sectional transmission electron microscopy (TEM) measurement [2] which showed the rod-like defect extended to the surface. Rapid thermal anneal (RTA) is effective to decrease the junction leakage current [2]. However, the problem is variation of junction leakage current in a wafer. This paper reports on the origin of the variation in junction leakage current and also reduction conditions of the variation when P ions were implanted at 1MeV with $1x10^{14}cm^{-2}$.

2. Experimental

After LOCOS formation, 1MeV P ions were implanted at the dose of $1x10^{14}cm^{-2}$ in p-(100) Si substrates. RTA was carried out for 30 seconds at a temperature of 1000-1150℃ with a ramp-up rate of 100-400℃/sec. BF_2 ions were implanted at 30keV with $3x10^{15}cm^{-2}$, followed by annealing at 900℃ for 10 minutes to fabricate p/n diodes. Junction leakage current was measured using p/n diodes with a area of 500um□, and the defects were evaluated by cross-sectional TEM measurement.

3.Results and Discussion

Figure 1 shows average junction leakage current at bias voltage of -5V, when RTA was carried out at a temperature ranging from 1000 to 1150℃ for 30 seconds with ramp-up rate of 200℃/sec. Average junction leakage current decreased at temperatures above 1050℃. However, the variation of junction leakage current is extremely large at 1050℃, as shown in Fig. 2. Typical feature for the variation of junction leakage current is the kink observed at a reverse bias voltage between -2 and -8V. Figure 3 shows the frequency of junction leakage current at -5V, obtained from 53 chips/wafer, using the same sample as Fig.2. The variation of junction leakage current was observed in about 30% chips in wafers. Figure 4 shows the standard deviation of junction leakage current at -5V for a ramp-up rate of 200 and 400℃/sec. Standard deviation of junction leakage current strongly depends on the annealing temperature and ramp-up rate, and it decreases according to the increase of annealing temperature and/or ramp-up rate. Standard deviation less than 20% was obtained at annealing temperature of 1100 and 1150℃ for ramp-up rate of 400 and 200℃/sec, respectively.

In order to clarify the origin of the kink in junction leakage current, the cross-sectional TEM measurement was carried out in the diodes with the kink in I-V curves, as shown in Fig. 2. Figures 5(a) and (b) show the cross-sectional TEM micrographs of the diodes with and without the kink in I-V curves, respectively. The defect observed in Fig.5 is identified to be dislocations which lay on an {110} Si plane . This dislocation was created from projective range (Rp) of P ions up to the depth of about 0.5um from the surface. Thus, this dislocation does not extend to the surface. The I-V curve indicates the kink at bias voltage of -4V, which corresponds to the depth of the dislocation position, measured by TEM. However, dislocation with small size existed around the Rp region as shown in Fig.5(b), when the kink was not observed in I-V curves.

Figure 6 summarizes the regions to show high junction leakage current, kink creation and low junction leakage current. At temperature below 1000℃, leakage current was high. At mediate region, kink was observed in I-V curves and variation was high, although the average current was low. At high temperature region, this is the only region to show the low leakage current with small variation. This result indicates that small variation is obtained at lower temperature for higher ramp-up rate. This seems to be caused by the competitive phenomenon between the defect formation related to diffusion of point defects during ramp-up in RTA and the anneal out of dislocation at maximum temperature in RTA. When RTA is carried out at higher temperature, dislocation size can be reduced. By increasing the ramp-up rate in RTA, dislocation size becomes smaller because of shorter time for dislocation formation. Therefore, dislocation can be annealed out or shortened at lower temperature, when ramp-up rate becomes higher.

These results indicate that ramp-up rate in RTA is very important for the defect formation.

4.Conclusion

The variation of junction leakage current was investigated, when P ions were implanted at 1MeV with $1x10^{14}cm^{-2}$. TEM measurement suggests that the origin of variation of leakage current is dislocation created from Rp of P ions to the depletion layer . The variation less than 20% can be obtained by RTA at high temperature (1100℃) with high ramp-up rate (400℃/sec) .

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References

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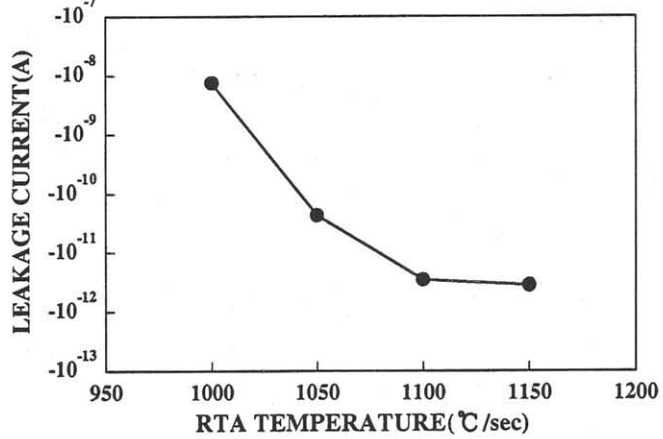

Figure 1 Average junction leakage current at -5V by RTA at temperatures of 1000 to 1150℃ for 30 seconds with ramp-up rate of 200℃/sec.

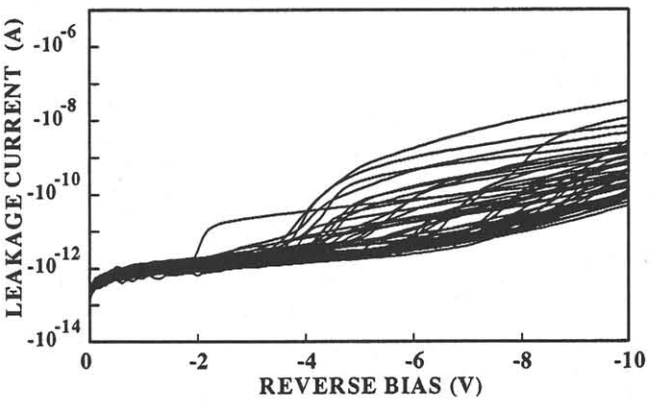

Figure 2 I-V characteristics of p+/n diodes in 53 chips/wafer at 1050℃ for 30 seconds with ramp-up rate of 200℃/sec.

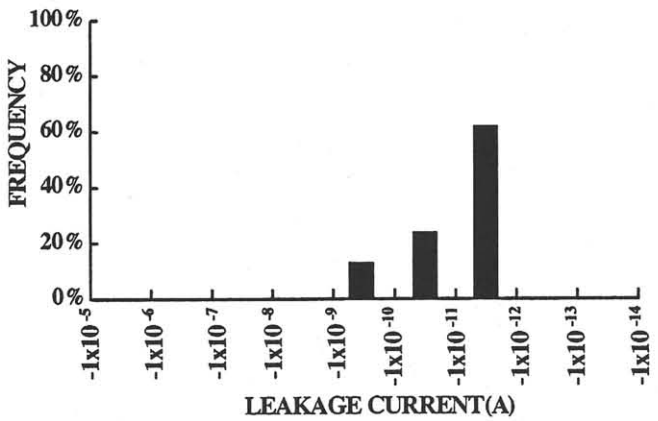

Figure 3 Frequency of junction leakage current at -5V, obtained from 53 chips/wafer , using the same sample as Fig.2

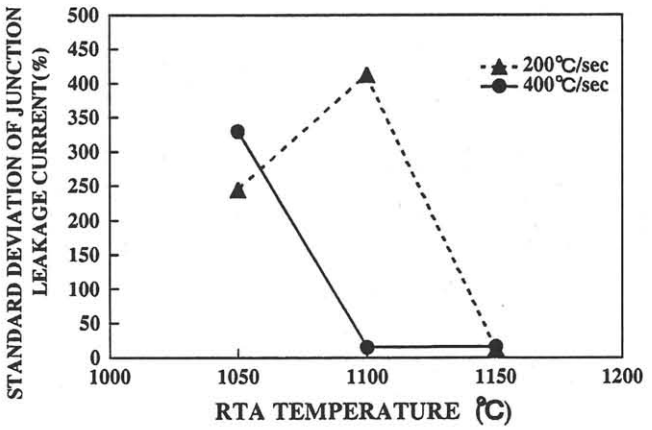

Figure 4 Standard deviation of junction leakage current at -5V.

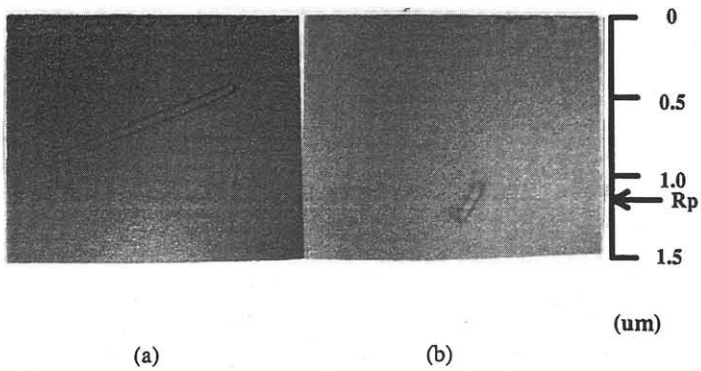

Figure 5 Cross-sectional TEM micrographs of diodes, with(a) and without(b) the kink in I-V curves.

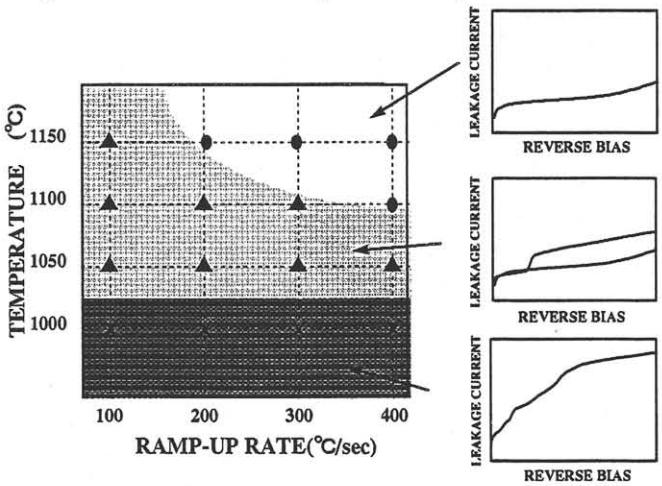

Figure 6 Summary of junction leakage current.