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Novel Ultra Clean Salicide Technology Using Double Titanium Deposited Silicide (DTD) Process for 0.1 μm Gate Electrode

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1. Abstract

We clarified that the fluorine contamination caused by gate side wall etching inhibits silicidation reaction and accelerates agglomeration. To overcome these problems, a novel "Double Ti Deposited silicide (DTD)" process has been developed. The key point of this process is deposition and subsequent removal of dummy Ti before silicidation. Contaminated Si and gate poly-Si surface layer caused by a reactive ion etching was perfectly removed and an ultra clean surface was obtained. As a result, low sheet resistance (3Ω/sq.) and thermally stable titanium silicide films were obtained in both n^+ and p^+ very fine 0.1μm gate.

2. Introduction

Self-aligned-silicide (Salicide) technology has become an essential part in fabrication of recent high speed CMOS logic LSI. $TiSi_2$ has been selected as a promising candidate for silicidation material because of its low resistivity and its higher manufacturability. However, $TiSi_2$ has following problems. 1) Thickness of the $TiSi_2$ film on highly doped n^+ -Si or -poly-Si is thinner than that on p^+ or undoped one. 2) When aiming for shrinkage of pattern dimension below the deep submicron gate level, phase transition (C49 to C54) failures and agglomeration occur at fairly low temperature annealing. As a result, sheet resistance increases. We recognized that these problems were mainly due to the presence of oxygen during the silicidation reaction in our previous study [1]. However, another contamination problem still remains. Fluorine contamination occurs due to direct exposure of the silicon and gate poly-Si surface to fluoride gas during the gate side wall etching. Little work is currently available for influence of the fluorine contamination. This study was carried out to reveal the influence of fluorine contamination on silicidation reaction and to develop a novel contamination free titanium silicidation process.

3. Influence of Fluorine

In our previous study, we proposed that one of the difficulties in achieving low sheet resistance of $TiSi_2$ could be attributed to recoil oxygen which was introduced during ion implantation through the cap oxide layer[1]. This issue was solved using a nitride instead of an oxide as an ion implantation cap layer [2] except for BF_2 ion implantation case. In the BF_2 ion implantation case, the sheet resistance of $TiSi_2$ was increased as dosages increased even in the oxygen free condition, as shown in Fig.1. This result indicates that the fluorine inhibits the silicidation reaction. Furthermore, it was revealed that the fluorine increased the reverse junction leakage current as shown in Fig.2. From these results, we concluded that elimination of the fluorine is necessary for obtaining stable silicidation reaction.

4. Double Ti Deposited Silicide Process

The fluorine contamination has been introduced during the gate side wall over-etching using a C-F based gas, even in the case of using boron as an acceptor implantation ion instead of BF_2. To obtain the damageless surface, the method of "dry + wet gate sidewall etching" or "only dry gate sidewall etching + Si chemical dry etching" was generally performed. However, in the former case, it was quite difficult to achieve precise sidewall width control in deep submicron regime, and in the latter case, removing the damage layer was insufficient because of termination of etching species on Si surface during the Si chemical dry etching. In order to ultimately remove the fluorine contaminated damage layer and to realize a contamination free silicidation, a "Double Ti Deposited (DTD) silicide" process has been developed. In this process, first dummy Ti deposition and subsequent removal are performed before second Ti deposition for silicidation. High reactivity of dummy Ti with Si substrate plays an important role for removing the damage layer. In this novel process, the contaminated damage layer react with dummy Ti and remove with dummy Ti before silicidation. Process condition is shown in Table 1.

5. Results and Discussion

Figure 3 shows standard deviation of Si surface roughness (R_{MS}) and AFM images before and after dummy Ti treatment (Ti deposition and subsequent removal). Si surface roughness (R_{MS}) was reduced from 0.34nm to 0.29nm by dummy Ti treatment. This result shows that the dummy Ti treatment did not degraded the Si surface flatness. Furthermore, it was confirmed that the dummy Ti was reacted with the Si by the sputtering energy[3] and substrate heating[4] as shown in Fig.4. This phenomenon is quite important to remove the contaminated damage layer. Figure 5 shows XPS spectra of fluorine on Si surface, and XPS intensity ratio of fluorine for silicon and that of Ti for Si in each process. It was revealed that the extremely large amount of fluorine existed on silicon surface in conventional treatment (condition A). This result shows that the conventional cleaning was not enough to remove the fluorine contamination before silicidation. In contrast to condition A, fluorine on Si surface was perfectly removed in process C. Furthermore, Ti peak was not found after dummy Ti removal. From these results, it was clarified that the dummy Ti treatment was quite effective for the fluorine removal on the Si surface. Figures 6 and 7 show the sheet resistances of $TiSi_2$ films formed on unpatterned Si and patterned poly-Si in each process. Impurity ions were not implanted and the first RTA was performed in very low temperature at 575°C to enhance the fluorine influence. The sheet resistances for A and B were higher than those of C and D as shown in Fig.6. This fact means that the increase of sheet resistance was caused by the presence of fluorine during the silicidation reaction. It seems that the fluorine inhibits the silicidation reaction. Furthermore, the fluorine influence became remarkable in narrower line width below 0.4μm as shown in Fig.7. From this result, it was clarified that the fluorine accelerates agglomeration. Figure 8 shows the sheet resistance of $TiSi_2$ on n^+ and p^+ gates as a function of gate length formed by the conventional, oxygen free and DTD (oxygen and fluorine free) processes. Low sheet resistances (3Ω/sq.) were achieved in extremely fine 0.1μm gate line width using the DTD process for both the n^+ and p^+ gate electrode.

6. Summary

It was clarified that the fluorine inhibits the silicidation reaction and accelerates agglomeration. Using novel DTD process, low sheet resistance (3Ω/sq.) and thermally stable silicide was achieved in both the n^+ and p^+ extremely fine 0.1μm gate, because of the perfect remove of fluorine contaminated damage layer using the dummy Ti treatment. This technology is expected to become important for the development of future deep submicron device.

Acknowledgments

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References

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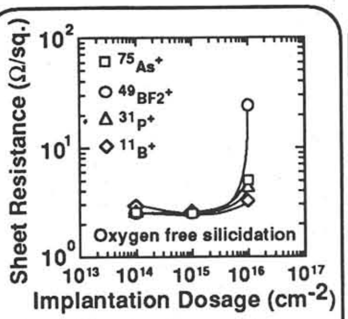

Fig. 1 Sheet resistance of unpatterned TiSi2 formed by oxygen free silicidation.

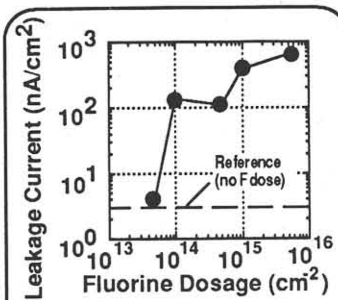

Fig. 2 Leakage current of TiSi2/n+/p junctions as a function of fluorine dosage.

Table 1 Surface treatment condition after gate sidewall etching.

A	Conventional (no dummy Ti depo.)	O_2 plasma+ H_2SO_4/H_2O_2+ NH_4OH/H_2O_2+ HF
B	DTD	Conventional treatment+ dummy Ti depo. (200°C) and removal
C	DTD	Conventional treatment+ dummy Ti depo. (440°C) and removal
D	Reference (no spacer etch)	HF only

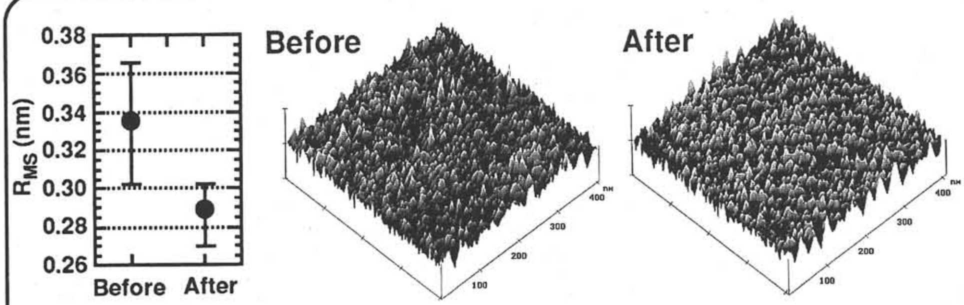

Fig.3 Si-surface roughness (RMS) and AFM images before and after dummy Ti deposition and removal.

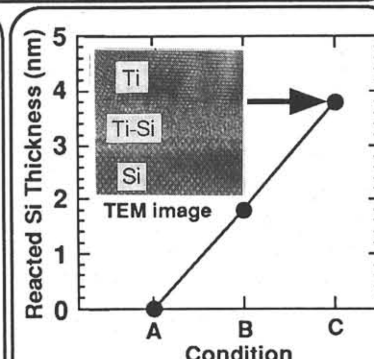

Fig. 4 Reacted Si thickness by dummy Ti deposition.

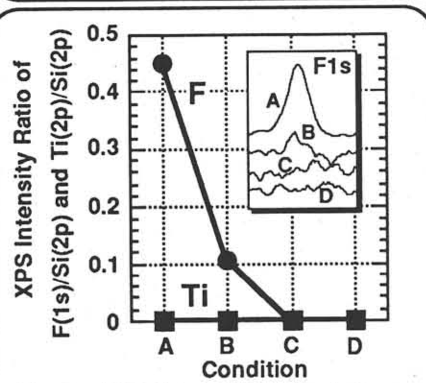

Fig.5 XPS intensity ratio between fluorine, titanium and silicon on the silicon surface for each condition.

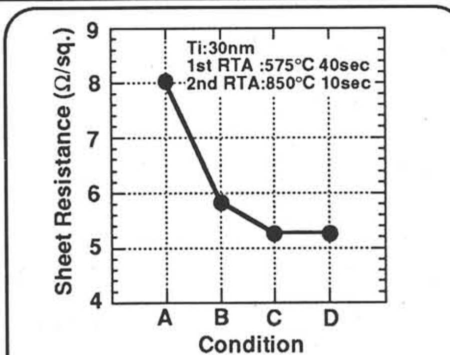

Fig. 6. Sheet resistance of un-patterned TiSi2 films on undoped Si for each surface treatment condition.

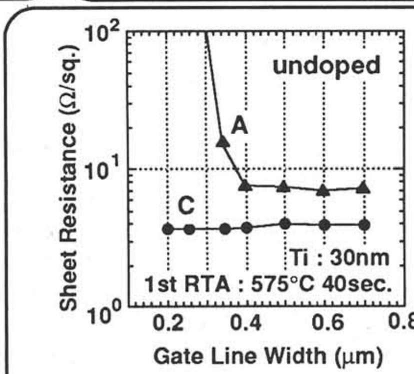

Fig. 7 Sheet resistance of TiSi2 on undoped poly-Si lines as a function of the line width.

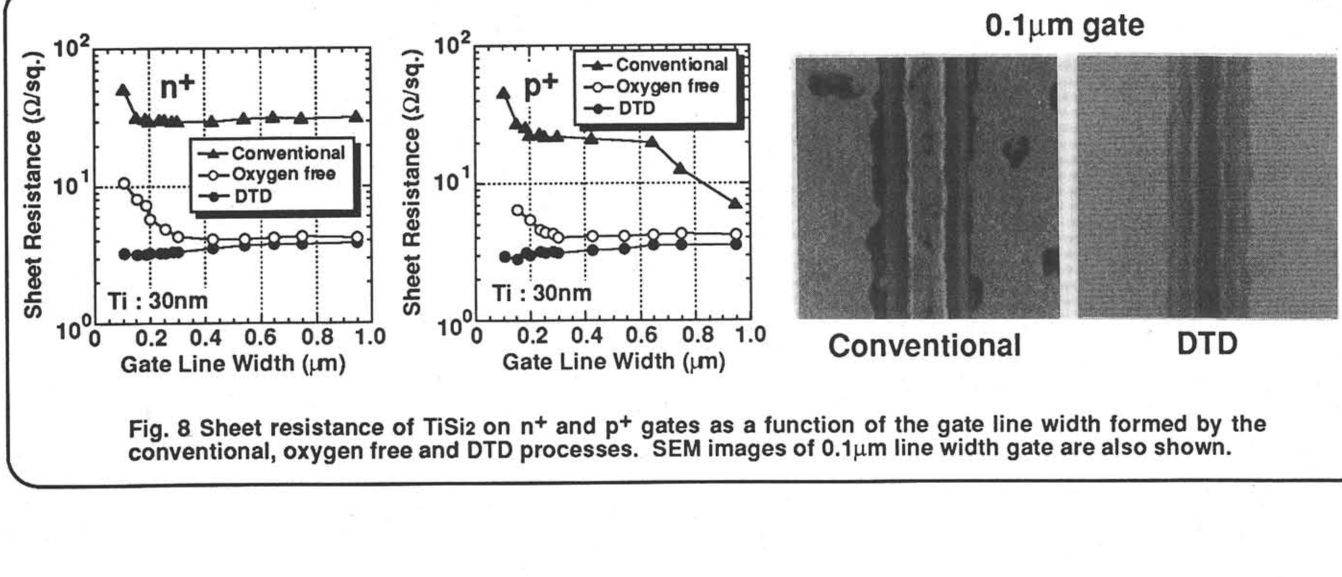

Fig. 8 Sheet resistance of TiSi2 on n+ and p+ gates as a function of the gate line width formed by the conventional, oxygen free and DTD processes. SEM images of 0.1μm line width gate are also shown.