Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 124-125

Self-Aligned 10-nm Barrier Layer Formation Technology for Fully Self-Aligned Metallization MOSFET

Hideki Matsuhashi, Akio Gotoh, Chang-hun Lee, Michio Yokoyama, Kazuya Masu and Kazuo Tsubouchi
Research Institute of Electrical Communication, Tohoku University,
Katahira 2-1-1, Aoba-ku, Sendai 980-77, Japan
Phone : +81-22-217-5532 Fax : +81-22-217-5533
E-mail matuhasi@riec.tohoku.ac.jp

1.Introduction

In deep-submicron MOSFET structure, parasitic resistances of source/drain and gate (S/D&G) regions limit the device performance. For the reduction of parasitic resistances, we have proposed a "Fully Self-Aligned Metallization MOSFET(FSAM-MOSFET)" using selective Al CVD technology (Fig.1).[1] The features are (1) SALICIDE for low Si/$TiSi_2$ contact resistances in S/D regions, (2) Self-aligned barrier layer on $TiSi_2$ surface, and (3) selective Al deposition on S/D&G regions for low sheet resistances. In this work, we report the self- aligned 10-nm barrier layer formation on SALICIDE n^+/p shallow junction for FSAM-MOSFET.

2.Self-aligned barrier layer formation

For the self-aligned barrier layer on the SALICIDE, Rapid Thermal Nitriding (RTN) process has been investigated.[2] However, RTN process requires a high temperature (≈1000°C). Furthermore, process wafer is exposed to air between RTN and the subsequent Al CVD process. The high temperature degrades the p/n shallow junction characteristics. The exposure to air easily causes oxidation of the barrier layer surface. The native oxide prevents the continuous Al growth because the Al CVD process is based on the surface electrochemical reaction on conductive materials.[3] The self-aligned barrier layer formation process should be a low temperature and in-situ process. Furthermore, the barrier layer should be as thin as possible. N_2 plasma nitridation[4] is expected to satisfy these requirements. In this work, self-aligned thin barrier layer in FSAM structure using N_2 plasma nitridation is developed.

3.Results and Discussion

$TiSi_2$ is formed using conventional SALICIDE process. $TiSi_2$ surface is pretreated with N_2 plasma in order to form the barrier layer. Typical conditions are P=0.2 Torr, N_2=100sccm, plasma power density=0.71W/cm^3. The substrate temperature (T_{sub}) is as low as 400°C. Without breaking the vacuum, CVD-Al is selectively deposited on $TiSi_2$ surface pretreated with N_2 plasma using DMAH [$(CH_3)_2AlH$][1] at 180°C.

[Selective Al deposition on nitrided layer]

Figure 2 shows SEM image of CVD-Al on the nitrided $TiSi_2$ surface. Al is selectively deposited on the nitrided $TiSi_2$ surface, and not on the SiO_2 surface. This means the selectivity of CVD-Al is maintained after the N_2 plasma nitridation.

[Barrier layer characteristics]

Figure 3 shows Si surface of (a) $TiSi_2$/CVD-Al and (b) $TiSi_2$/nitrided-layer/CVD-Al. These samples are annealed at 400°C/N_2/30min. before the removal of $TiSi_2$/CVD-Al layer. No pits are observed on the Si surface with the N_2 plasma nitridation. Figure 4 shows I-V curves of n^+/p shallow junction (a) without and (b) with the N_2 plasma nitridation. The n^+/p shallow junction with the N_2 plasma nitrided barrier layer has no leak current after the annealing at 450°C/N_2/30min. Therefore, it is confirmed that the nitrided layer on $TiSi_2$ acts as a barrier layer for Al.

[Characterization of 10-nm Ti-Si-N barrier layer]

Figure 5 shows the XPS spectra of (a)N_{1s}, (b)$Ti_{2p3/2}$ and (c)Si_{2p} on $TiSi_2$ surface pretreated with the N_2 plasma. N_{1s} peak is clearly observed on $TiSi_2$ surface in (a). In (b), $Ti_{2p3/2}$ contains Ti-N bonding peak (455.0 eV). In (c), Si_{2p} peak also contains Si-N bonding peak (100.5 eV). So that, the $TiSi_2$ surface after the N_2 plasma treatment is Ti-Si-N ternary compound. Figure 6 shows TEM image of the cross section of $TiSi_2$/Ti-Si-N layer/CVD-Al. The thickness of Ti-Si-N layer is about 10nm. Electron diffraction pattern of the Ti-Si-N layer is halo. This means the Ti-Si-N layer is amorphous phase. It is concluded that the barrier layer on $TiSi_2$ formed by the N_2 plasma is 10-nm Ti-Si-N ternary amorphous layer.

It has been reported that 100nm Ti-Si-N amorphous layer acts as a barrier layer for Al.[5] In this work, **10nm** Ti-Si-N amorphous layer is found to act as a barrier layer for Al.

4.Summary and Conclusion

The self-aligned 10-nm barrier layer formation on SALICIDE n^+/p shallow junction has been developed. It has been experimentally confirmed that (1) Aluminum is selectively deposited on the nitrided layer on $TiSi_2$, (2) the low temperature N_2 plasma nitrided layer acts as a barrier layer for Al, (3) This barrier layer is 10-nm Ti-Si-N ternary amorphous layer. The combination of SALICIDE, the N_2 plasma nitridation and the selective Al CVD is promising for fabricating deep-submicron FSAM-MOSFET.

References

1) K.Masu, et al : VLSI Technol., Digest of Technical Papers, in Honolulu, 1996 p.44.
2) M.Yokoyama, et al.,Abs. Spring Meeting, Jpn.Soc. Appl. Phys.,30p-K-10(1995) (in Japanese)
3) K.Masu, et al : Applied Surface Science 79/80 (1994)237-243.
4) M.Sekiguchi, et al.,Abs. Spring Meeting, Jpn.Soc. Appl. Phys.,26-pQ-4(1996) (in Japanese)
5) X.SUN, et al : Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, p.401.

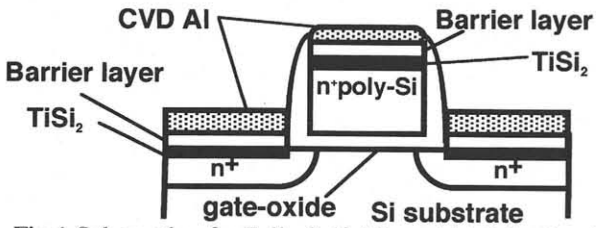

Fig.1 Schematic of a Fully Self-Aligned Metalization MOSFET.

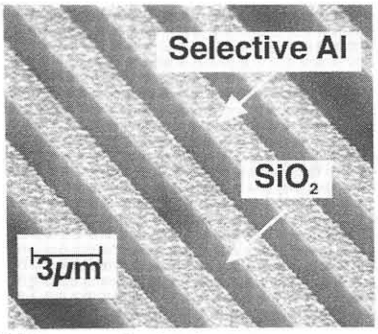

Fig.2 SEM image of selectively deposited Al on nitrided $TiSi_2$ surface. Al is deposited using DMAH at 180°C.

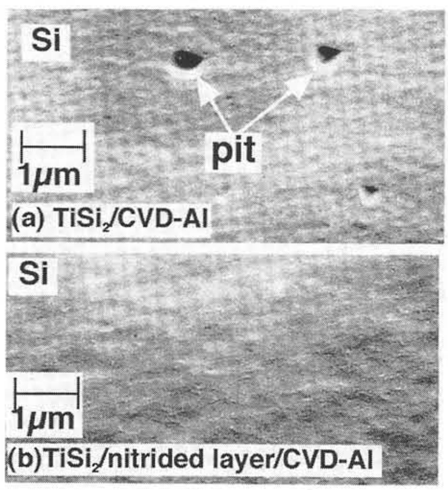

Fig.3 Si surface of (a) $TiSi_2$/CVD Al and (b) $TiSi_2$/nitrided layer/CVD Al.

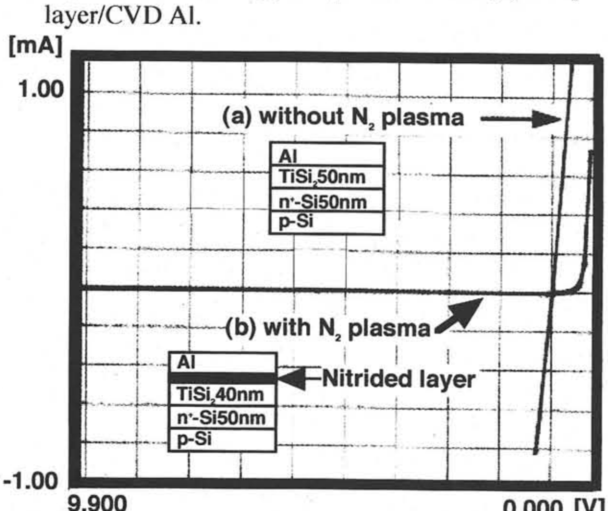

Fig.4 I-V curves of n^+/p junction (a) without and (b) with N_2 plasma nitridation. Contact pattern size is $10\times10.\mu m^2$. Samples are annealed at 450°C/N_2/30min.

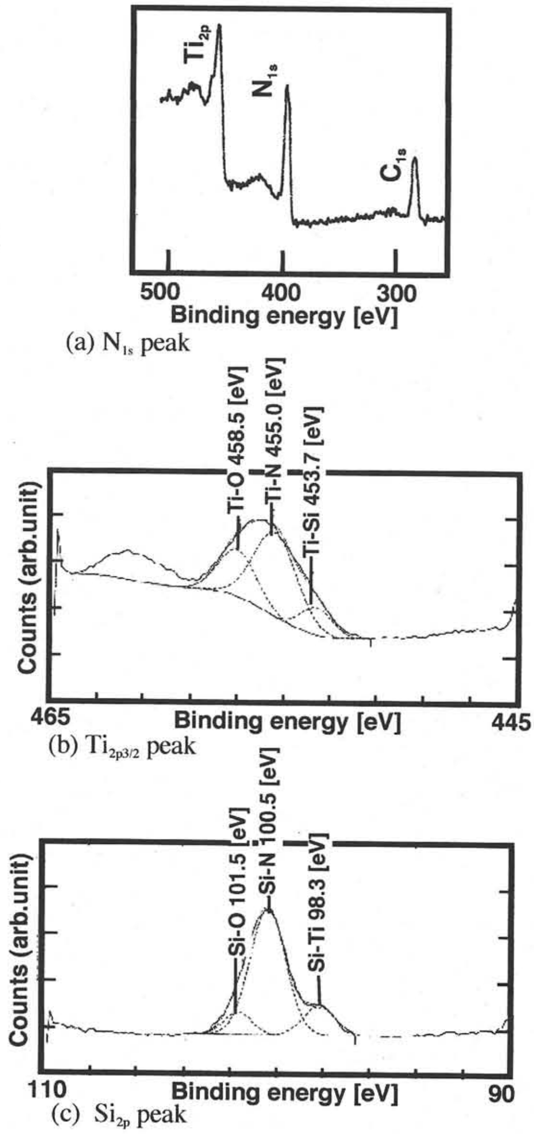

Fig. 5 XPS spectra of (a)N_{1s}, (b)$Ti_{2p3/2}$ and (c)Si_{2p} on $TiSi_2$ surface pretreated using N_2 plasma.

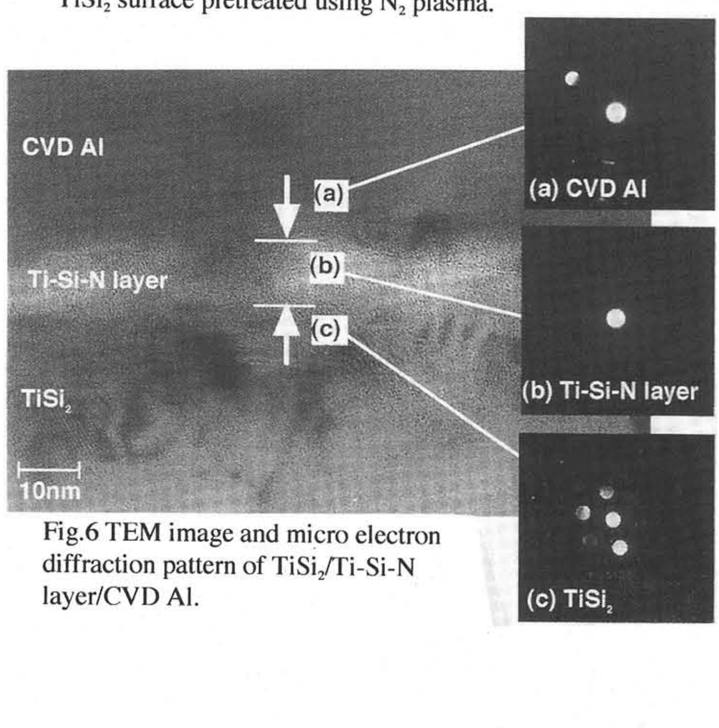

Fig.6 TEM image and micro electron diffraction pattern of $TiSi_2$/Ti-Si-N layer/CVD Al.