

Improvement of Bit-Line Contact Resistance for Memory Devices with Silicide Gate

T. H. Kim, Y. J. Choi, C. Y. Moon, H. C. Koh, J. H. Jin, and B. I. Ryu

DRAM Product Engineering, Memory Business, Samsung Electronics

Kiheung-Eup, Yongin-City, Kyungki-Do, Korea 449-900

(TEL) 82-2-760-7842, (FAX) 82-2-760-6649/6855, (E-Mail) jjin@khpost.semi.samsung.co.kr

1. Introduction

The polycide word-line (WL) commonly used in today's memory devices has a shortcoming that when a contact for bit-line (BL), another polycide layer, is formed on the WL, the interfacial contact resistance between the two polycide layers becomes large. This is, as depicted in Fig. 1, known due to the dopant redistribution; the phosphorus ion in the BL poly (BP) outdiffuses into adjacent (i.e., upper/lower) silicide and possibly WL poly (GP) layers during the subsequent heat cycles [1]. Obviously, such an increase of contact resistance is a big obstacle for next generation DRAMs, because it not only increases the RC time delay significantly, but also reduces the so-called "low Vcc margin". Although there have been many researches to solve this problem, they have limited utility. In this paper, we present a novel process, featured by a BL contact built with SiON spacer on its sidewall, which could "phenomenologically" eliminate the silicide layer on top of the WL, thus realizing more conductive poly-on-poly instead of poly-on-silicide structures. In addition, our experimental data show that the spacer also helps to reduce the leakage current between the BL and WL, and to improve the dynamic refresh characteristics.

2. Experimental Results

The idea is based on the fact that WSi easily reacts on nitrogen component commonly found in an ARL (Anti-Reflective Layer), and thus its sidewall is removed away slightly. Its implementation was done on a 16M DRAM process with a minimum feature size of 0.29 μ m whose highlights are well illustrated in Fig. 2. After the definition of the WL, the HTO (High Temperature Oxide) and BPSG layers are deposited in a conventional way, and then BL contacts (a.k.a. DC = Direct Contact) are patterned on both the WL and active regions. Afterwards, a proper amount of SiON layer is deposited on the entire wafer, and etched away anisotropically to form the spacer on the sidewall of the contacts. During this process, the silicide on top of WL is removed

away as evidenced in Fig. 3, thus enabling the poly-on-poly structure whose contact resistance is significantly lower than that of poly-on-silicide structure. Note in Table I that active contact resistances remain almost the same, but that the DC resistance is decreased by about a factor of three compared with the normal process. Such a phenomenon is, as described before, believed to be related to the reaction of the WSi layer on the nitrogen component in the SiON spacer (The full mechanism is under study). We also note that the statistical variation is diminished a lot regardless of the contact type, which we believe implies that the actual contact size is, relatively speaking, not sensitive to the cleaning process thanks to the etch-resistant spacer.

Another advantage for the DC spacer is that it improves the dielectric margin between the BL and WL significantly, because it prevents the contact hole from becoming large (see Fig. 2(b)), which otherwise occurs because the interlayer dielectric (usually BPSG) is etched laterally during the post-contact cleaning processes. Thus, the leakage current for the SiON spacer is, as shown in Fig. 4, decreased by about two orders of magnitude compared with the conventional case (Assessment of the correlated low Vcc margin is still underway). Of course, this kind of scheme increases the contact overlap margin, eventually widening the photo-process window. In point of product performance on the other hand, dynamic refresh characteristics are improved, because isolation distance between the BL and storage node contacts is increased by the spacer thickness itself. According to our experimental data, the spacer of 350Å improves the dynamic refresh margin in terms of the 10th bit failure by around 25 %, as shown in Fig. 5.

3. Summary

We developed a viable process which can reduce the contact resistance between two polycide layers by a factor of three. In addition, experimental data based on a 16M DRAM process show that the BL to

WL leakage current level is lowered by two orders of magnitude, and that the dynamic refresh characteristics are also improved by about 25%.

Reference

1) P. Pan and N. Hsieh, "Dopant Diffusion in Tungsten Silicide," *J. Appl. Phys.*, 53(4), April, 1982.

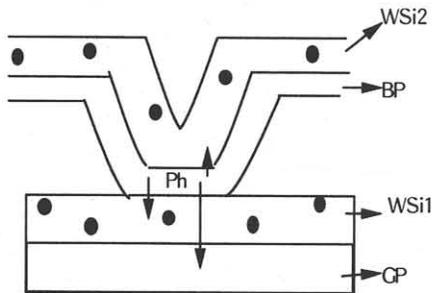


Fig. 1 : Dopant redistribution model.

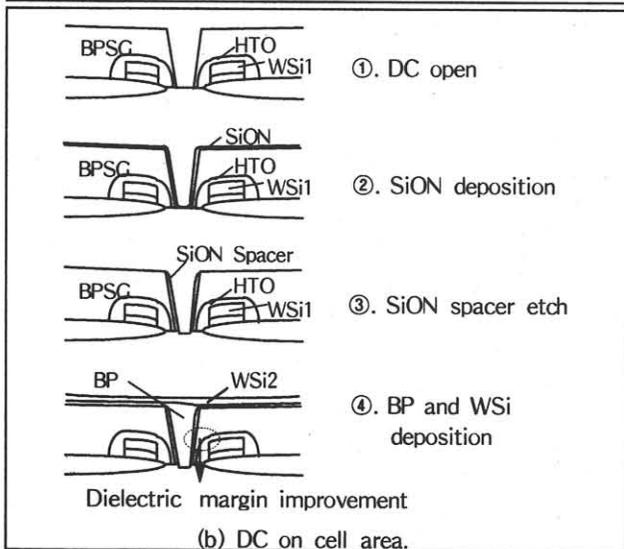
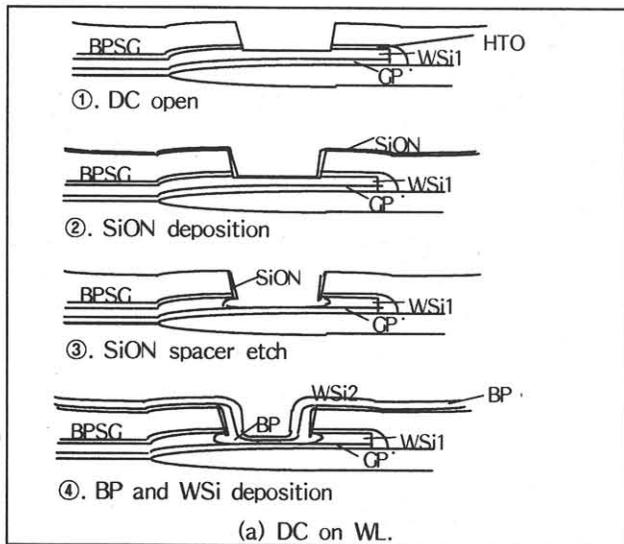
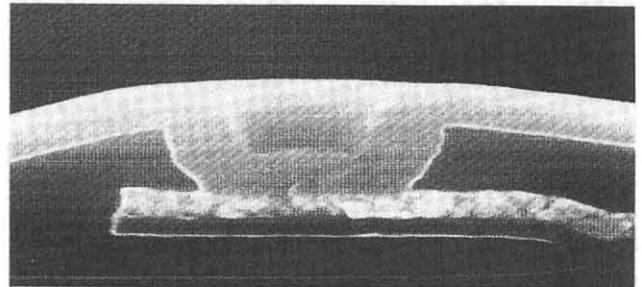


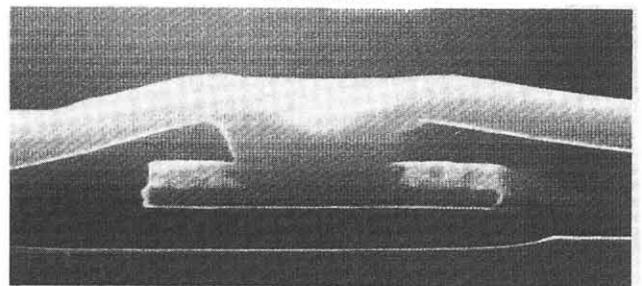
Fig. 2 : Schematic diagram of key steps.

Table I : Comparison of DC resistances.

Unit : Ω /contact	Normal		This work	
	avg.	3σ	avg.	3σ
Cell	388.7	346.3	341.5	232.3
BP/N+	172.1	105.4	153.7	56.7
BP/CP	310.9	217.8	111.1	91.1



(a) normal.



(b) this work.

Fig. 3 : SEM photograph of DC on WL.

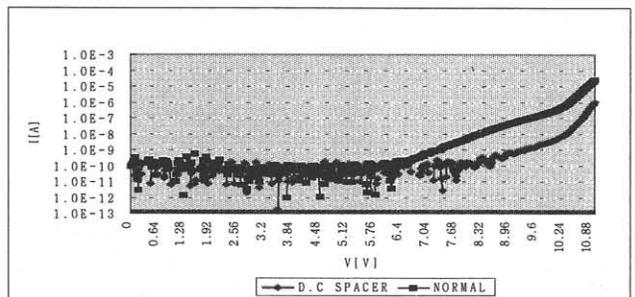


Fig. 4 : HP 4156 plot for leakage currents between WL and BL (83°C).

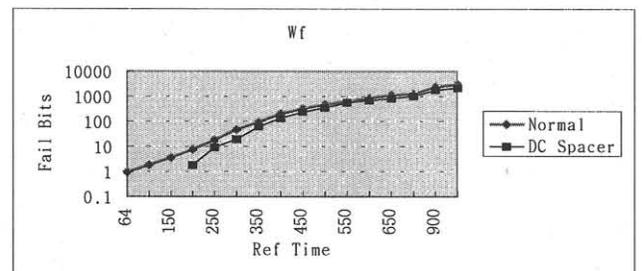


Fig. 5 : Cumulative fail bits as a function of dynamic refresh time (83°C).