Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 268-269

Invited

Stacked Capacitor DRAM Cell Technology

Kuniaki Koyama

ULSI Device Development Laboratory, NEC
1120, Shimokuzawa, Sagamihara, Kanagawa, 229-11, Japan
Phone/Fax: +81-427-79-9921/+81-427-71-0938, E-mail: kkoyama@lsi.tmg.nec.co.jp

1.Introduction

DRAM cell size has decreased to approximately $0.25um^2$[1] due to the development of lithographic technologies and the change from planar capacitor cells to three dimensional capacitor cells. In this paper, I would like to discuss problems in capacitor technology and cell contact technology for future gigabit stacked capacitor DRAM cells.

2.DRAM Technology Trend

Table1 shows a DRAM technology trend in memory cell size and design rule (DR) and minimum pitch (F). Gigabit DRAM cell size is predicted lower than $0.32um^2$. The minimum storage capacitance of the DRAM cell is determined by the sense amplifier sensitivity, data retention time, the immunity of soft errors. It has remained above approximately 25fF/cell in even in gigabit scale DRAM generations.

In stacked capacitor DRAM cell technology there are two key technologies to reduce cell size. One is the capacitor technology concerning the combination of capacitor structure and capacitor film. The other is the memory cell contact technology concerning the reduction of overlay margin between cell contact and word/bit line.

3.Stacked Capacitor Technology

Fig.1 Shows several types of stacked capacitor structures. Fig.2 shows equivalent silicon oxide thickness (Toxeff) versus the dielectric film thickness at several dielectric constants. Oxidized nitride (ON) has mainly been used in DRAM cell. Higher dielectric constant materials such as tantalum oxide (Ta2O5) and barium strontium titanate (BaxSr1-xTiO3) have been studied [2,3,4].

Box type is a very simple structure, but the projected area of stack electrode becomes smaller as cell size becomes smaller. The side area is much larger than the top area, but the stack electrode height is limited by lithography due to depth of focus (DOF). An electrode height of 1.1um is necessary for a capacitor film with 1.5nm Toxeff as shown in Fig.3. Global planarization of interlayer insulator film avoids the problem of DOF but causes another problem of the enlargement of peripheral metal contact aspect ratio as shown in Fig.4. To overcome the problem a new metal technology such as CVD metal or addition of local interconnect layer [5,6] is required.Prior to using of these technologies, Semi-global planarization of interlayer over capacitor is suitable for such high stack electrodes.

The problem of cylinder structure is caused by the limitation of cylinder thickness. Fig.5 shows the relation between stack electrode width and stack electrode inner width. If both sizes need 0.05um from the point of mechanical strength and plate electrode coverage, cylinder structure could not be applied in 0.10um rule. Cylinder type is promising by application of Ta2O5 and metal electrode [7] above 0.13um rule as shown in Fig.6.

Hemi Spherical Grain (HSG) technology can adapt box type and cylinder type capacitors with silicon electrode . But high dielectric constant material using metal electrode cannot be applied. So the minimum Toxeff is 2.5nm now. Box+HSG type needs above 0.7um height of stack electrode for 0.18um rule as shown in Fig.7 [8]. By contrast, Cylinder+HSG needs 0.6um height even for 0.13um rule.

The problems of application of high dielectric constant film are reduction of leakage current, improvement of coverage of film, and fine patterning of metal electrode. Especially the first and second problem are very important. Even if leakage current becomes small by increasing film thickness, increase of capacitance cannot be expected because thick dielectric film would be buried in the small space between stack electrode before plate electrode formation. In planar type with 0.10um rule, a Toxeff of below 0.07nm which means the dielectric constant is above 2700 for a film thickness of 50nm.

4.Cell Contact Technology

Small contact hole patterning has become difficult as compared with line and space patterning in lithography. The memory cell size is determined as wiring width and space, contact size and overlay margin. Overlay margin is important factor as shown in Fig.8. Therefore, several self-align contact and pad processes have been proposed [9,10,11]. They enlarge the alignment margin between word line and cell contact. The future problem is how to enlarge alignment margin between bit line and capacitor node contact.

5.Conclusion

In stacked capacitor DRAM cell, cylinder and HSG structure is promising above 0.13um rule, and higher dielectric constant film is probably used below 0.18um rule. But below 0.1um rule, cylinder process cannot be used and Toxeff of capacitor film will be needed below 0.8nm (BOX type) or 0.07nm (Planar type) and cell contact will be formed self-aligned to both word and bit lines.

References

1)H.Koga et al.:IEDM Tech. Dig. (1996) p589
2)Y.Takaishi et al.:IEDM Tech. Dig. (1994) p839
3)S.Kamiyama et al.:IEDM Tech. Dig. (1993) p49
4)H.Yamaguchi et al.:IEDM Tech. Dig. (1996) p675
5)K.Itabashi et al.:VLSI Tech.Dig. of Tech. Papers (1997) p21
6)J.Y.Lee et al.:IEDM Tech. Dig. (1996) p593
7)J.M.Drynan et al.:VLSI Tech. Dig. of Tech. Papers (1997) p151
8)K.N.Kim et al.:VLSI Tech. Dig. of Tech. Papers (1997) p9
9)H.Hada et al.:IEDM Tech. Dig. (1995) p665
10)S.P.Sim et al.:IEDM Tech. Dig. (1996) p597
11)K.Sunouchi et al.:IEDM Tech. Dig. (1996) p601

Table1 DRAM Technology Trend

	64M	256M	1G	4G	16G
Design Rule (um)	0.35	0.25	0.18	0.13	0.10
Minimum Pitch (um)	0.45	0.30	0.20	0.15	0.12
Cell Size (um2)	1.62	0.72	0.32	0.18	0.105

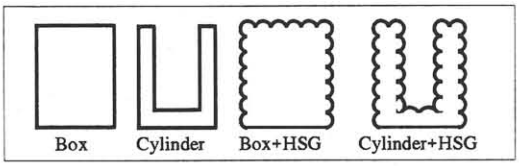

Fig.1 Several types of stacked capacitor structures

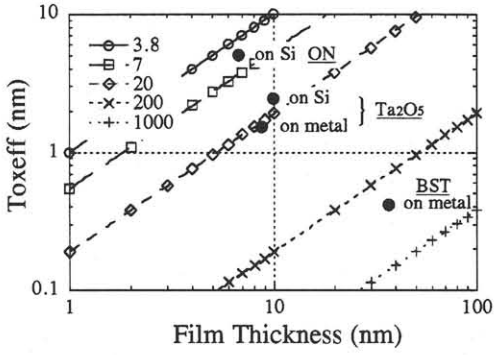

Fig.2 Toxeff vs. dielectric film thickness at several dielectric constants

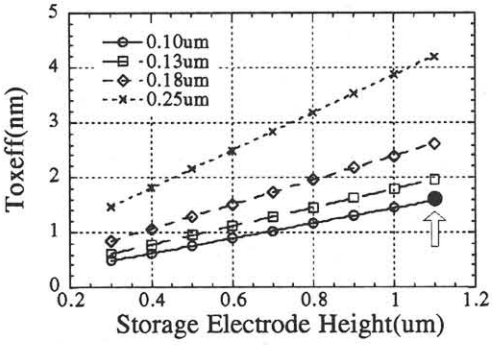

Fig.3 Calculation value of BOX type structure for several design rules

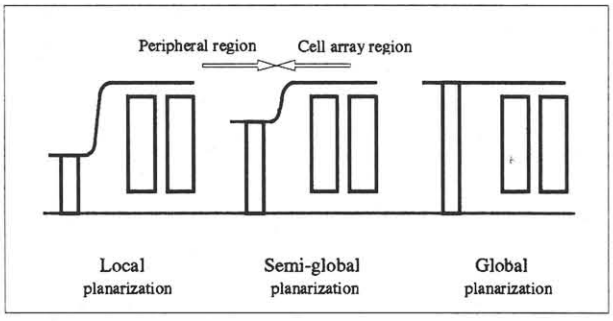

Fig.4 Three levels of planarization of interlayer over stacked capacitor

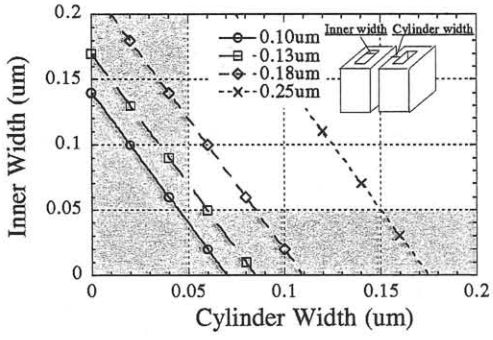

Fig.5 Inner width dependence of cylinder width in the direction of bit line

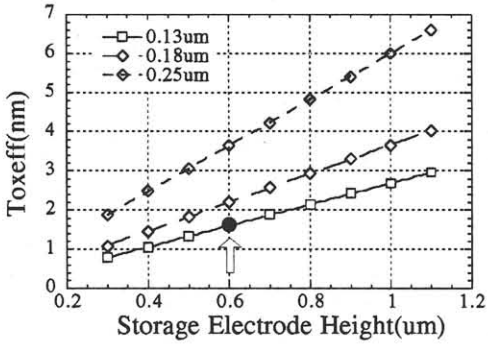

Fig.6 Calculation value of Cylinder type structure for several design rules

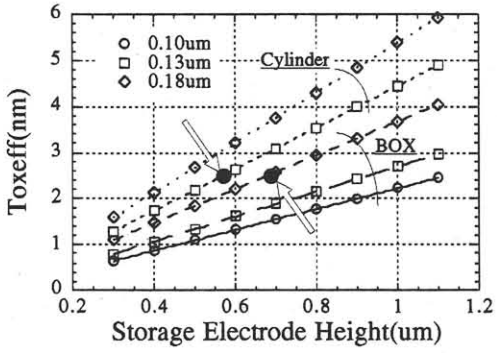

Fig.7 Calculation value of HSG type structure for several design rules

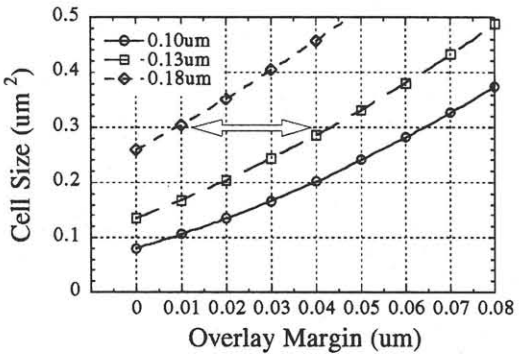

Fig.8 Memory cell size dependence of overlay margin between cell contact and word/bit line