Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 270-271

Invited

Trench Capacitor DRAM Technology for 256Mb and Beyond

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1. Introduction

With the scaling of minimum dimensions to 0.25μm and below, DRAM technology faces a number of new challenges. System requirements for higher bandwidth between memory and processors necessitate faster transistor performance. System on a chip applications with embedded DRAM push performance even further and also require added levels of wiring. From the technology perspective, the cell structure is rapidly approaching wiring limited sizes, leading to very aggressive scaling of lithography to maintain the rate of cell area reduction. This means pushing 248nm DUV lithography down to 0.18μm with relatively small depth of focus. This paper describes a 0.25μm trench capacitor dram technology that was developed to meet these challenges. The scaling of this technology down to 0.18μm is also discussed.

2. Cell Structure

The cell described in this work (Figure 1) is a BuriEd STrap cell or BEST for short [1]. It is a variant of the Substrate Plate Trench Cell [2], where signal is stored on the inside of the trench as opposed to the traditional trench cell where signal is stored on the outside [3]. This overcomes the disadvantages of the traditional trench capacitor cell with trench to trench punchthrough eliminated since the substrate region between trenches is at a common potential. Data retention and soft error rate immunity are very good since the cell junction area is small and the cell is constructed inside a well which blocks the collection of charge generated in the substrate. Key features are complete self alignment, large storage capacitance, and an integration sequence that insures local and global planarity throughout the process [4].

Self alignment is achieved in two ways. As shown in Figure 2, the buried strap connection from the trench capacitor to the array transistor is created through the interaction of the shallow trench isolation with the capacitor. The capacitor is formed first and a sidewall connection is formed along the entire perimeter of the trench. Subsequently the shallow trench isolation removes this connection on all trench surfaces except where the connection to the transistor is desired [1]. The bitline contact to the transistor is self-aligned through a process that etches SiO_2 with high selectivity to Si_3N_4. These two processes lead to a cell size of 0.605μm^2 at 0.25μm dimensions, with a cell size of 0.245μm^2 projected for early 1Gb designs.

3. Technology Integration

With the continued optimization in optical lithography, process integration must deal with smaller and smaller useable depth of focus. This trend is shown in Figure 3, where the maximum allowable topography to be able to print minimum pitch wiring is shown as a function of technology generation. Estimates of topography created during trench capacitor cell formation and stacked capacitor cell formation are included for comparison. It is clear that planarization must be included as a standard technique throughout the process in order to continue using optical lithography. Typically, chemical mechanical polishing is used for planarization of trench capacitors, shallow trench isolation, contact studs, insulators over gates, and damascene wiring levels [4].

The advantages of this integration scheme can be seen in Figure 4. Even after three levels of wiring (tungsten bitline and two levels of aluminum) the surface is quite flat. This is promising for future embedded dram applications, where the logic portions of the chip will require extra levels of metal. The lack of high temperature processing after transistor formation offers opportunities for higher performance transistor design as well.

4. Challenges in Scaling to 1Gb

The BEST cell concept is scalable to 1Gb dimensions without major changes. Recent work has shown that through proper control of the deep trench etching and scaling of the nitride/oxide dielectric thickness to the range of 4-5nm, one can achieve capacitance of >35fF at 1Gb dimensions [5]. As seen in Figure 5, trench etch rate drops slowly as dimensions drop from 0.7μm to < 0.2μm. Profiles are well controlled even to the smallest dimension. This ability to achieve large capacitance values without the introduction of new materials into manufacturing is very attractive. By scaling all features to minimum dimension, a cell size of 0.245μm^2 is attainable [6].

5. Conclusions

Despite many challenges, trench capacitor cells will be used in the 1Gb era and beyond. Features such as shallow trench isolation, damascene wiring, and transistors appear to scale well, especially considering the opportunity for reduced thermal cycles offered by the trench integration sequence. There are concerns about array device design since off current requirements are very severe in DRAMs [6], but they appear manageable. Trench cells offer the advantage of allowing the continued use of conventional NO dielectrics into the 1Gb generation and an inherently planar integration sequence.

Acknowledgements

The author thanks the IBM DRAM Development Team for creating a challenging and rewarding work environment, along with colleagues from Siemens and Toshiba who contributed to this work.

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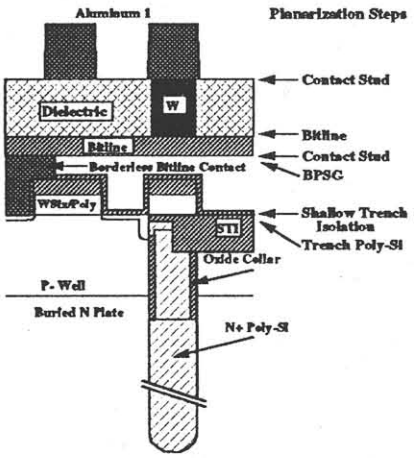

Figure 1. BEST Cell for 256Mb DRAM [1].

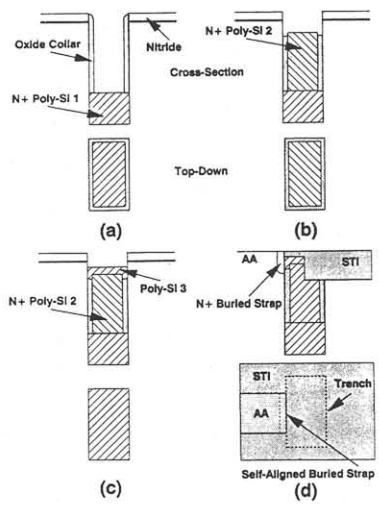

Figure 2. Schematic cross-section and top views showing formation of buried strap connecting trench and active area.

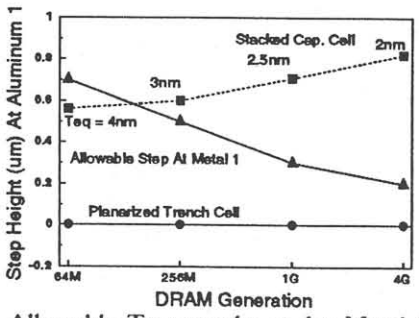

Figure 3. Allowable Topography at 1st Metal from 64Mb to 4Gb

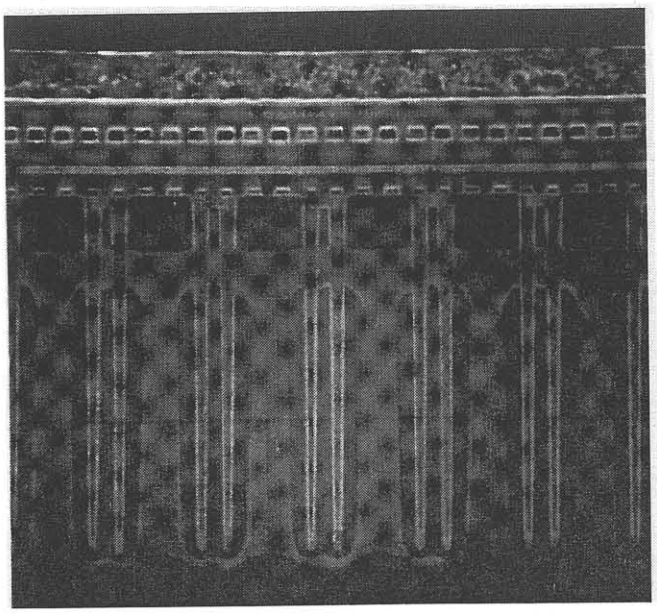

Figure 4. Highlighted SEM cross-section of BEST cell array.

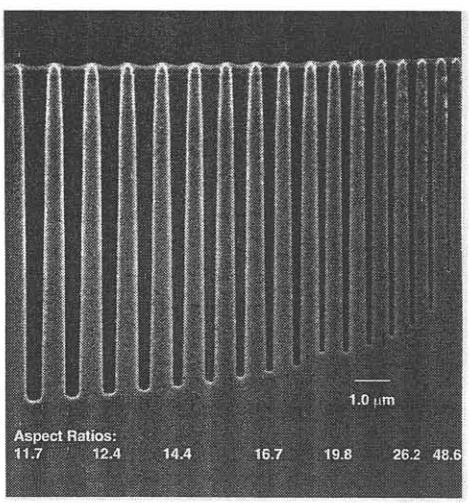

Figure 5. SEM cross-section of test wafer showing trench depth for varying trench sizes.