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A Process Integration of (Ba, Sr) TiO_3 Capacitor into 256M DRAM

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1. Introduction

As the integration density of DRAM increased up to 1 giga bit, obtaining capacitance for operation of the devices become more and more difficult. Conventional dielectric material, SiN/SiO_2 and Ta_2O_5 combined with HSG, are now actively being studied for 256M DRAM. However, there is still a question about whether these processes can be adaptable to the DRAMs with higher integration densities than 1G. (Ba,Sr)TiO_3 (BST) dielectric material with noble metal electrodes attracts major interest in the DRAM industry owing to its very large dielectric constant.[1,2,3] However, process integration issues, including the electrode material, barrier layer and cross-contamination, are still not cleared although the dielectric material itself has been proved to be applicable to DRAM. Currently, electrode process, such as material and fabrication technique, is mainly focussed because the integration scheme is largely determined by the selection of the electrodes. Noble metal electrodes, such as Pt, have a merit of very small leakage current density although their etching is difficult. Conducting oxide electrodes, such as RuO_2, have a merit of easy etching although the leakage current level is very high. In both cases, the barrier layer which protects the electrode from the reaction with poly-silicon plug poses the main integration problem because the barrier layer must be remained conductive after the processing.

In this study, fabrication and electrical characterization results of an integrated BST capacitor having Pt electrodes with 256M density are presented.

2. BST capacitor fabrication.

A schematic flow diagram of the BST capacitor fabrication process is shown in Fig.1. A 500-nm-thick undoped SiO_2 layer was deposited on 6" (100) Si wafer which had conducting surface layer made by As^+ implantation. Then, contact holes were opened and a 300 -nm-thick P-doped poly-Si layer was deposited. Contact plugs were formed by CMP of the poly-Si layer. Ti-silicide layer was selectively formed and barrier layer was deposited. Then, Pt electrode layer was sputtered with 100-nm or 200-nm-thickness. SiO_2 hard masks were formed on the Pt-layer by the photolithographic process. Pt storage nodes with 0.58㎛-pitch and 256 M density were formed by a MERIE-type dry etching process with $O_2/Cl_2/Ar$ gas chemistry. After removing the mask, a low temperature SiO_2 layer was deposited on the Pt nodes and etched-back to form the side wall spacer. The SiO_2 etching process was carefully controlled to maximize the exposed storage node area. A standard metal cleaning process was done prior to the BST deposition and the BST thin films were rf-sputter-deposited at wafer temperatures over 400℃ to 500℃ with a 40-nm-thickness. Then, a 100-nm-thick plate Pt electrode was formed. Some of the fabricated capacitor were post-annealed at 550℃ for 10 min. under N_2 atmosphere. The electrical parameters were measured by a HP-4155A and HP-4284.

3. Results

Figure 2 shows cell capacitance (C_s) and dielectric loss (D) of the capacitor before and after the post-annealing. The BST films were deposited at 400℃ and 450℃ on 100-nm-high storage nodes having TiN barrier and no SiO_2 spacer. With increasing the deposition temperature, C_s increases due to the improved crystalline quality. However, D greatly increases with the temperature owing to the oxidation of the TiN barrier. After the post-annealing, C_s of the 400℃ sample increased by more than 4 times compared to the as-fabricated state but C_s of the 450℃ sample does not increase al all. D of both of the two capacitors have a common value of about 0.4 after the annealing. The variation of Cs and D should be understood from the combined effect of BST crystallization and the barrier oxidation. Figure 3 shows the equivalent circuit diagram explaining the increase of BST capacitance and dielectric loss due to the barrier oxidation as the heat treatment proceeds. The barrier oxidation drastically increases D and eventually reduces the C_s. To prevent the barrier layer from the oxidation, three types of parameters are changed; SiO_2 spacer was formed to cover the barrier on the side wall area, TiN was changed to a new barrier material which is more resistant to the oxidation, and the Pt storage node height was increased to 200 nm. The results are summarized in Fig. 4. The new barrier material withstands the oxidizing atmosphere during the BST deposition without being oxidized up to 450℃. Adding the SiO_2 spacer increases the temperature up to 510℃ by prohibiting direct exposure of the barrier to the atmosphere. Increasing the storage node height suppresses the oxygen diffusion through the storage node as well as increasing the storage node area and the C_s. The maximum C_s obtained from the 20 0-nm-high storage node without any post-annealing is about 28fF/cell with D of about 1.5%. Cross-sectional SEM micrograph of the integrated capacitor is shown in Fig. 5. A capacitance-voltage (C-V) plot of the capacitor is shown in Fig. 6. By a post-annealing under N_2 atmosphere C_s is increased to 36fF/cell at 0 bias without increasing D. C_{min}/C_{max} over -1V to 1V is about 94%. Excellent leakage current characteristics of the integrated capacitorare shown in Fig. 7. The leakage current after the mild post-annealing at 1.5 V is of order of 0.1 fA/cell, which is low enough for the stable operation of the device. The leakage currents at 85℃ and 1.5 V are still less than 1 fA/cell although these data are not presented here.

To increase the C_s the space between storage nodes were minimized by control of the exposure during the

photolithographic process and the spacer etching process was optimized. In this case, a maximum C_s of 72 fF/cell with a leakage current density of about a few fA/cell were obtained after the post-annealing.

4. References

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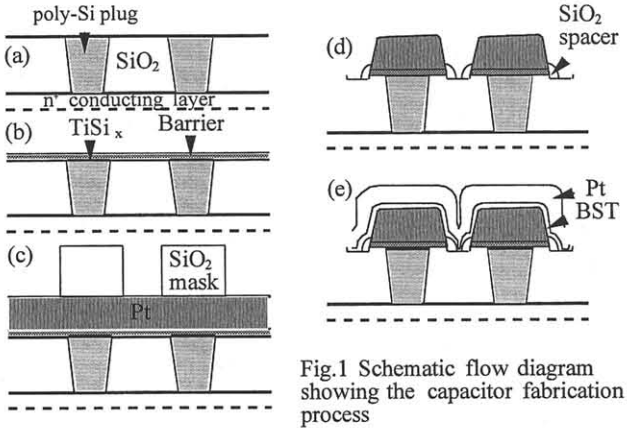

Fig.1 Schematic flow diagram showing the capacitor fabrication process

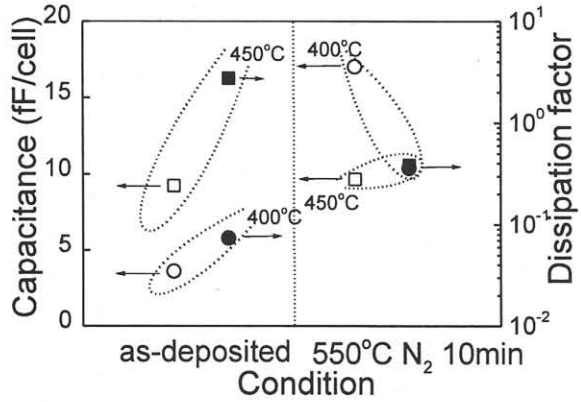

Fig. 2 Variations of C and D before and after post-annealing

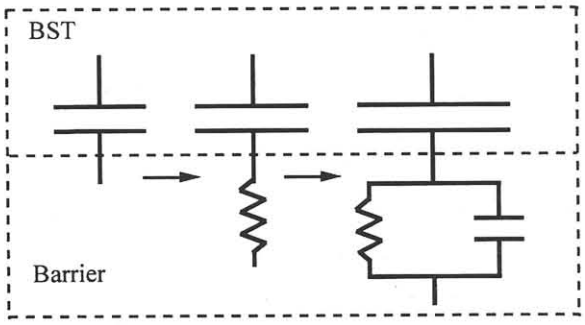

Fig. 3 Equivalent circuit diagram of the integrated capacitor showing the barrier oxidation

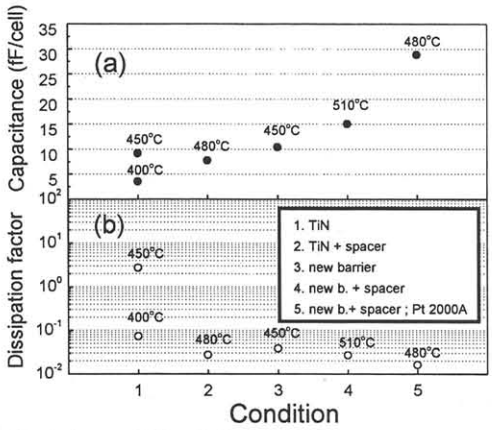

Fig. 4 Variations of C and D by various process parameters.

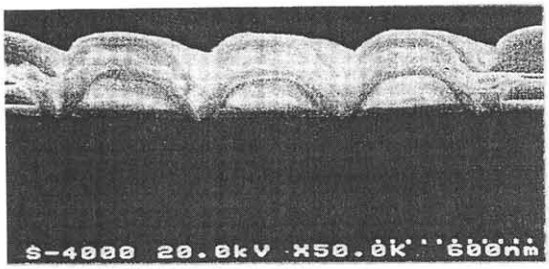

Fig. 5 SEM micrograph of the integrated capacitor

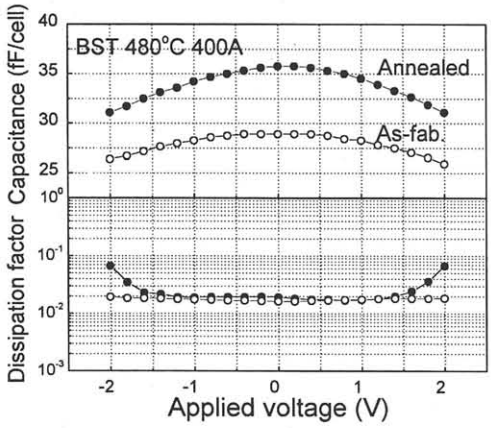

Fig. 6 Variations of C and D as a function of bias voltage.

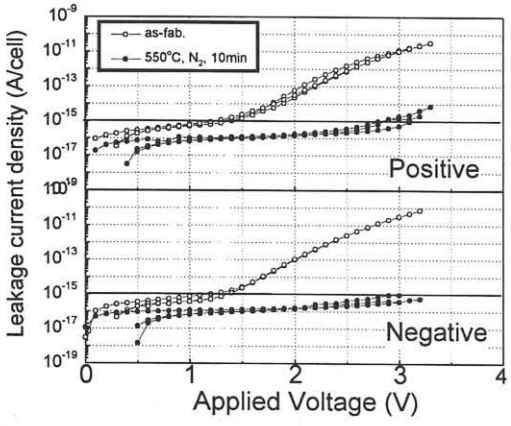

Fig. 7 Variations of J_L as a function of applied voltage.