Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 276-277

Invited

Flash Memory Technological Survey for Future Scaling

Natsuo AJIKA, Hirokazu MIYOSHI

Mitsubishi Electric Corporation ULSI Laboratory
4-1, Mizuhara, Itami, Hyogo 664, Japan
Phone: +81-727-84-7368, FAX: +81-727-80-2693, E-mail: ajika@lsi.melco.co.jp

1. Introduction

Flash memory market is growing favorably in the 0.5 μm era and now they are penetrating into 0.35 μm. On the other hand, market demand for cost reduction and voltage reduction to flash memory seems to be stronger and stronger rather than other memories. This is because that two of the largest markets for flash memory, those are code storage of mobile systems and file storage such as memory cards, are the most aggressive fields for those two requirement.

According to the situation, this paper describes the future scaling issues of flash memories (cost, voltage and so on) from the technological stand point of view.

2. Cost Scaling

As is well known, cost reduction of semiconductor memories directly means the chip size reduction.

Fig. 1 shows the schematic illustration of typical flash and DRAM cell layouts assuming the alignment margin as f/2 (f: minimum feature size). It can be seen that the cell area of the flash should be half of DRAMs' by using the same process technology and alignment criterion.

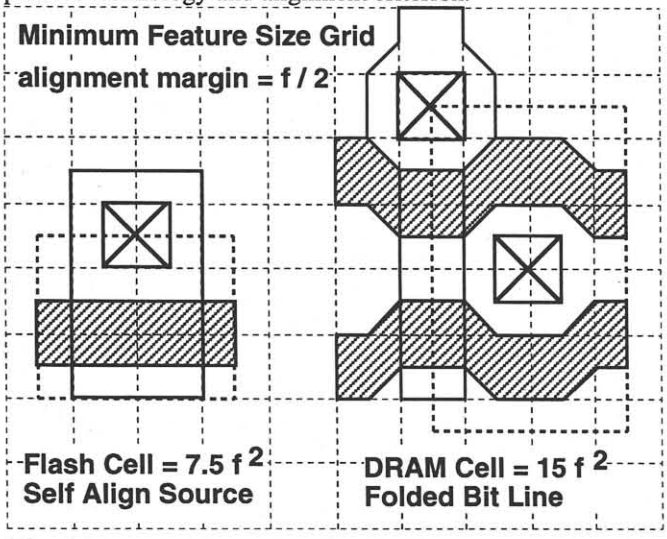

Fig. 1 Schematic illustration of typical layouts of flash memory and DRAM cells. Grid lines indicate the minimum feature size 'f' and alignment margin is assumed to be f/2.

Fig. 2 shows the normalized chip size/ bit (chip size/ bit/ f^2) vs. density of now shipping DRAMs and flash memories. Cell occupancy to the whole chip of both DRAMs and flash memories are estimated to be about 50 to 60%. Normalized cell size (cell size/f^2) under the assumption of alignment margin as f/2 is $15f^2$ for DRAMs as mentioned before. In the case of flash memories those of NOR/DINOR, NAND and AND cells are $7.5f^2$, $6f^2$ and 6 to $8f^2$ respectively.

Comparing above estimation to fig. 2, it seems that normalized cell size of actual DRAMs have already achieved smaller value than $15f^2$. This is because that the DRAM process has been improved on the alignment margin and/or contact hole diameter.

On the other hand, normalized cell size of flash memory of NOR type is 10 to $12f^2$ [1]. This indicates there still remains some room to reduce the cell size. In the case of the flash memories for file storage, those are NAND [2], AND [3], Multi Level Cell [4][5] and so on [6], good scaling results comparable to DRAMs have been achieved. (fig. 2)

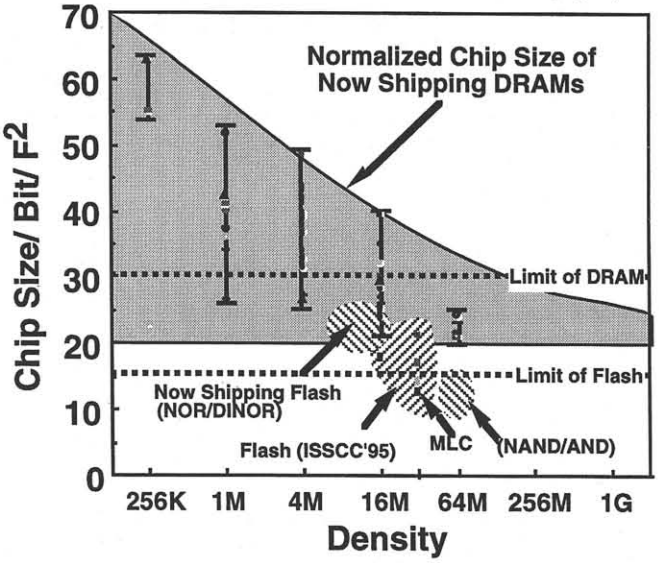

Fig. 2 Normalized chip size/ bit vs. density of now shipping DRAMs and Flash memories.

Let us consider the ideal cell layout of flash memories for code storage. A flash memory cell consists of one channel region, 1/2 contact hole, 1/2 source diffusion and 1/2 isolation. Fig. 3 indicates the schematic cell layout of an ideal flash cell, that is all the inactive elements are formed by self-aligned manner (self-align contact [7], self-align source and self-align isolation [8-10]). In this case, cell area could

be reduced to $4f^2$ theoretically. $4f^2$ is the smallest limit for one element under the minimum feature size of f, so that this is really an ultimate cell layout.

This kind of cell layout degrades the cell coupling ratio, in consequence it degrades some kind of cell performances. Some kind of coupling ratio enhancing technology [11] will be required to utilize self-align isolation process.

The other subjects to be solved to realize a full self-align cell are, to maintain isolation ability, source line resistance and contact resistance. In the case of CHE-NOR, high isolation ability, low contact and source line resistance are needed because of its high current flow needed during CHE operation. On the other hand, DINOR [12] operation does not need much, so that DINOR potentially has big advantage for future cell scaling.

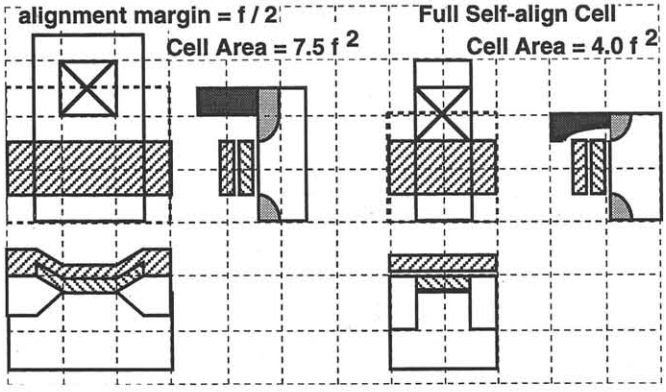

Fig.3 Schematic cell layout of the ideal flash memory cell (right hand side). All the inactive elements are formed by self-align manner.

3. Power Scaling

Power dissipation and supply voltage reduction is another demand for flash memories, especially flash memories for code storage. In particular, power dissipation during read is the most concern because read mode is the most frequent operation. The issue is word line voltage scaling during read. Word line voltage during read is restricted by Vt distribution of low state and number of cells connected to a bit line [13]. So that the intentional Vt distribution control for low state [14] and some kind of divided bit line array architecture should be needed for power and voltage scaling. Otherwise, word line boost scheme is required [15] to scale supply voltage, and it may consume excessive power and cause some delay in data access.

4. Subjects for Other Scaling

Other important scaling issues including performance improvement such as high speed read out, high program through put [16][17] and periphery scaling will be described at the conference.

5. Conclusion

NOR type flash memories have not scaled enough compared to DRAMs.

Self-align process technology of the inactive elements is very effective for flash memory scaling, because of flash cell consists of only one active element and many room for alignment margin. Furthermore this kind of cell reduction does not need to proceed lithography generation and does not cause any side effects such as reliability degradation.

References

1) T. Nakayama, et al., "A 60ns 16Mb Flash EEPROM with Program and Erase Sequence Controller", ISSCC '91, p.260.
2) K. D. Suh, et al., "A 3.3V 32Mb NAND Flash Memory with Incremental Step Pulse Programing Scheme", ISSCC '95, p.128.
3) A. Nozoe, et al., "A 3.3V High Density AND Flash Memory with 1ms/512B Erase & Program Time", ISSCC '95, p.124.
4) M. Bauer, et al., "A Multilevel-Cell 32Mb Flash Memory", ISSCC '95, p. 132.
5) T. S. Jung, et al., "A 3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Application", ISSCC '96, p.32.
6) R. Cernea, et al., "A 34Mb 3.3V Serial Flash EEPROM for Solid-State Disk Application", ISSCC '95, p.126.
7) Y. Zhang, et al., "Fluorocarbon high density plasmas. VII. Investigation of selective SiO2-to-Si3N4 high density plasma etch processes", J. Vac. Sci. Tech. A 14(4), 1996, p.2127.
8) Y. S. Hisamune, et al., "A 3.6μm2 Memory Cell Structure for 16Mb EPROMs", IEDM '89, p. 583.
9) S. Aritome, et al. "A 0.67μm2 Self-aligned Shallow Trench Isolation Cell for 3V-only 256Mbit NAND EEPROMs", IEDM '94, p. 61.
10) M. Kato, et al., "A Shallow-Trench-Isolation Flash Memory Technology with a Source-Bias Programming Method", IEDM '96, p. 177.
11) H. Shirai, et al., "A 0.54μm2 Self-Aligned, HSG Floating Gate Cell (SAHF Cell) for 256Mbit Flash Memories", IEDM '95, p.653.
12) H. Onoda, et al., "Improved Array Architectures of DINOR for 0.5 μm 32M and 64Mbit Flash Memories", IEICE Trans. Electron., E77-C, No. 8, 1994, p. 1279.
13) K. Yoshikawa, "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design", Sympo. on VLSI Tech. '96, p.240.
14) S. Kobayashi, et al., "A 3.3V-Only 16Mb DINOR Flash Memory", ISSCC '95, p.122.
15) A. Baker, et al., "A 3.3V 16Mb Flash Memory with Advanced Write Automation", ISSCC '94, p.146.
16) T. Ohnakado, et al., "Novel Electron Injection Method Using Band-to-Band Tunneling Hot Electron for Flash Memory with a P-channel Cell", IEDM '95, p. 279.
17) O. Sakamoto, et al., "A High Programming Throughput 0.35μm P-channel DINOR Flash Memory", Sympo. on VLSI Tech. '96, p. 222.