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An Optimized Via Contact Scheme of FeRAM for Double-Level Metallization and Beyond

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An optimized via contact scheme has been investigated at double-level metal process for the 64k ferroelectric RAM. Aluminum reacts easily with platinum during the post-anneal when Al has a direct cotnact with the top Pt of the ferroelectric capacitor. This reaction deteoriorates the property of the ferroelectric capacitor, and also results in the failure of a cell opertion. To prevent this reaction, TiN barrier layer was introduced as the barrier layer. This contact scheme showed the good properties of ferroelectric capacitor up to 400℃, which indicated TiN acts as the good diffusion barrier at via for the double-metal process.

1. Introduction

Ferroelectric random access memory (=FeRAM) has heen investigated due to nonvolatility, high speed, and low voltage operation. It has the great potential for replacing DRAM, SRAM, Flash Memory[1]. Recently, several research group reported that they had developed FRAM device using PZT thin film. They consists of a 2T/2C cell and a single-metal, which require the larger chip area than the 1T/1C cell array and multi-level metal scheme[2]. In multi-level metalization, the contact between Al and Pt serving as the top electrode is required as shown in figure 1. The good contact is very important to get a reliable cell operation at the ferroelectric RAM.

This study focused on optimizing the via contact scheme for the electrically stable ferroelectric capacitors at FeRAM. Several barrier schemes such as Ti,TiN/Ti, and TiN barrier layer have been investigated for the best contact scheme of the 64K FeRAM in which double metal scheme is used.

2. Experiments

As shown in figure 1, a unit cell has a 1T-1C cell structure and a double-metal configuration. The capacitor was stacked over BPSG, which consists of a Pt/PZT/Pt/TiO_2 stack structure. The capacitor area was 9 μm^2. PZT thin film was coated by sol-gel method and then annealed at 650℃ for 30 min. in oxygen ambient for crystallization. TiO_2 capping layer and ILD(inter-layer dielectric) were deposited on the capacitor subsequently. 1T-1C FeRAM was completed after Via and metal 2 formation.

In this experiment, we have prepared four different samples. One was that metal 2 Al directly deposited on Pt top electrode, the others were that TiN, TiN/Ti, and Ti barrier layers were inserted into the inteface between metal 2 and top Pt. To investigate the stable Pt/Al contact scheme during post annelaing step, samples were annealed at 200℃, 300℃, and 400℃ in air respectively. The reaction of the contact of Pt/Al after post-annealing was evaluated by hysteresis loop, I -V curve and SEM cross section, AES depth profile.

3. Results and Disscusion

Figure 2 shows the hysteresis loops of the samples that metal 2 Al was directly deposited at the top Pt electrode. The characteristics of the curve started to be degradated at 300℃ and dramatically degradated at 400℃.

Figure 3 shows the SEM cross-sectional views of these samples. Pt layer still remained at 200℃, while Pt was completely consumed due to the reaction at 300℃. The reaction layer became thicker and IMD oxide was destructed because of the stress resulted from the volume expansion after annealed at 400℃. Pt is able to absorb Al easily due to its solid solubility, and Pt makes many metallic coumpounds with Al easily in Pt-Al phase diagram[3].

Figure 4 shows the AES depth profile of the sample deposited at 25℃ and annealed at 400℃, respectively. The result reveals that there is Al-rich Pt-Al compound at the Al surface and Pt-rich phase at the Pt/PZT interface after annealed at 400℃.

Figure 5 shows the I-V curves of Pt/PZT/Pt capacitor at two different polarities. After annealed at 200℃, there was no big difference on the two kinds of the leakage currents at two different polarities, at which Pt layer is still remained, even it reacts as shown at the figure 3(b). But, the leakage current was abruptly increased after annealed at 300℃, when a positive bias was applied to the bottom electrode, indicating the top electrode and PZT interface to be conductive by the change of the contact from Pt/PZT to Pt-Al coumpoud/PZT. At 400℃, both interfaces were degraded severely. The increase of the leakage current of negative polarity (top electrode is ground, bottom electrode positive) resulted from severe reaction between the top Pt and Al. However, the increase of positive polarity leakage current is thought to be due to differnt mechanism such as the degradation of bottom electrode interface caused by the stress resulted from the volume expansion of the compound of the Pt/Al as shown in figure 3(d).

To prevent those reactions with the stable interfaces between Al/Pt, TiN, TiN/Ti, and Ti diffusion barrier were introduced. Figure 6 shows the hysteresis loops of the PZT capacitors with various barrier layers. The sample with TiN barrier shows good hysteresis loop, while the others with Ti, TiN/Ti barrier are degraded. The degradation is due to the diffusion of Ti into PZT layer through Pt[4].

Figure 7 shows the hysteresis loop of the capacitor with TiN barrier. No degradation has been observed up to 400℃, and their properties were superier to the sample without TiN. The leakage currents of the samples with and without TiN as a function of annealing temperature at 10V are shown in figure 8. Even though the leakage current of the sample with TiN was increased at 400℃, which was much lower than that of the sample without TiN. Figure 9 and 10 shows SEM cross-section and AES depth profile of the sample with TiN barrier respectively. TiN barrier layer remained and no reaction was observed after annealed at 400℃. These results indicate that TiN acts as a diffusion barrier for Al/Pt contact. It is expected that TiN would be a promising diffusion barrier for the multi-metallization scheme.

4. Conclusion

An optimized Via contact scheme has been investigated at double-level metal process for the 64K FeRAM. The sample without diffusion barrier showed severe reaction between Pt/Al during the post-annealing. The reaction causes the degradation of the electrcial properties of the ferroelectric capacitor. The TiN barrier scheme between Al and Pt has been introduced. This scheme showed the good properties of capacitor up to 400℃ and it is a promising candidate for the Via contact for high density FeRAM.

5. References

[1].Tanabe, et al *Sympostum on VLSI Technology Digest of Technical papers* (1995) 123,
[2].J.T.Evans, et al, *IEEE Journal of Solid State Circuit*, **23**, (1988) 1171
[3].E.A.Brandes, et al, *Smithells Metsls Reference Book*, pp.11 -46
[4] Bruchhaus, et al, *Mater.Res.Soc.Symp.Proc.* **243**, (1993)123

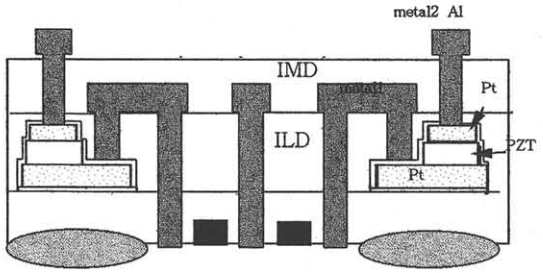

Fig.1 Double metal FRAM structure

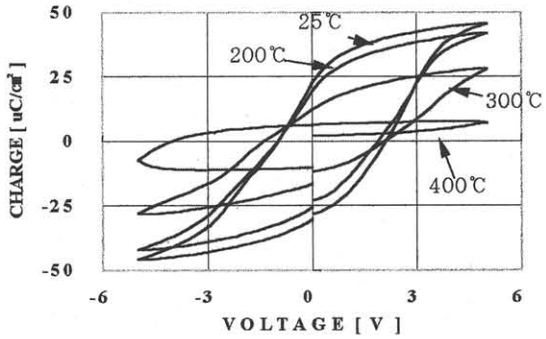

Fig.2 Hysteresis loop of PZT without barrier as a function of post-anneal temperature

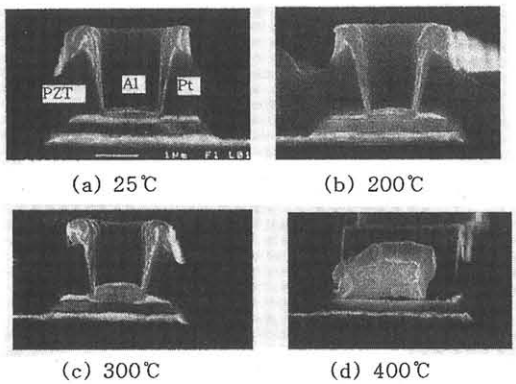

Fig.3 SEM cross section of PZT capacitor without barrier as a function of post-anneal temperature

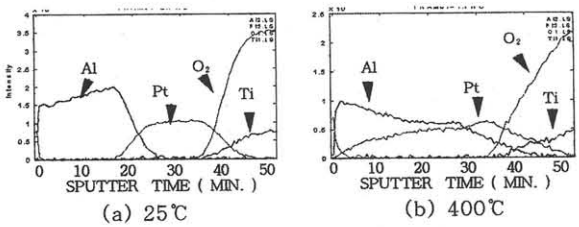

Fig.4 AES depth profile of Al/pt/PZT/Pt

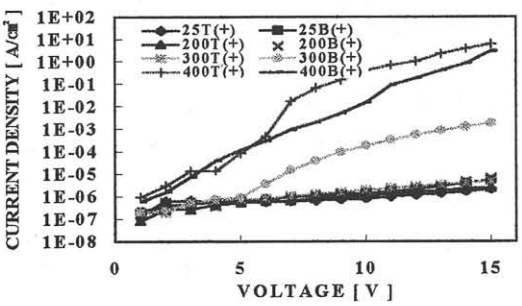

Fig.5 I-V characteristics of PZT without barrier layer

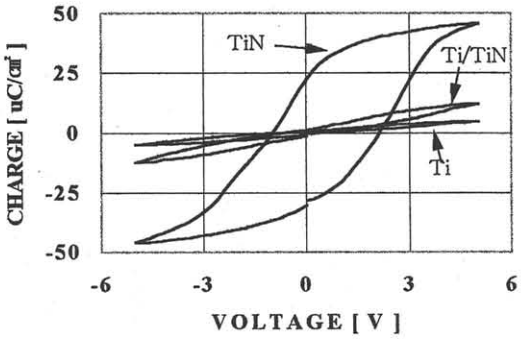

Fig.6 Hysteresis loop of PZT with various barrier between top Pt/Al

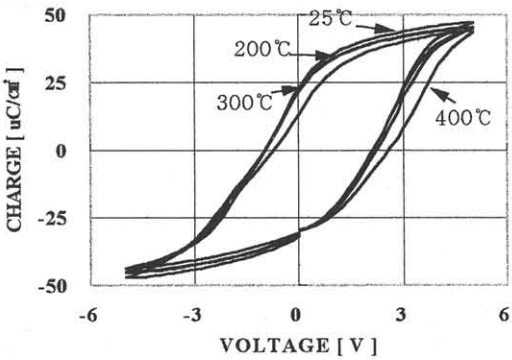

Fig.7 Hysteresis loop of PZT with TiN barrier as a function of temperature

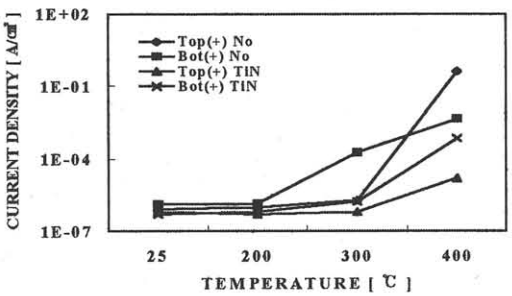

Fig.8 Leakaage current of PZT with and without TiN as a function of temperature at 10V

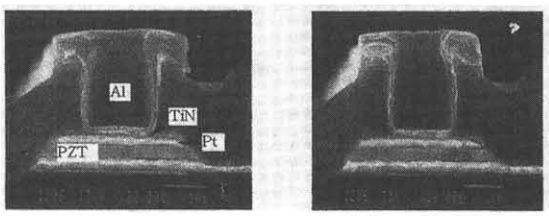

Fig.9 SEM cross section of PZT capacitor with TIN barrier layer

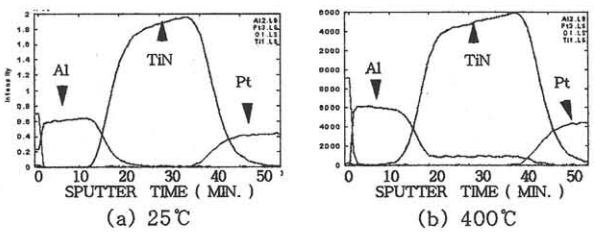

Fig.10 AES depth profile of Al/TiN/Pt