Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 32-33



# A Proposal of $Pt/SrBi_2Ta_2O_9/CeO_2/Si$ Structure for Non Destructive Read Out Memory Devices

Dong Suk Shin , Yong Hee Han , and Yong Tae Kim[1]

[1]Semiconductor Materials Laboratory, Korea Institute of Science and Technology, Seoul 136-791
Phone/Fax: 82-2-958-5745/82-2-958-5739, E-mail: ytkim@kistmail.kist.re.kr
Korea Department of Materials Science, Korea University, Sungbukgu, Seoul 136-701, Korea

## 1. Introduction

Recently, non volatile ferroelectric random access memory(NV-FRAM) devices have been a focus of future device technology[1,2]. At present, there are two ways for NV-FRAM; one is the DRO (destructive read out) type that consists of a transistor and a capacitor. Another one is the NDRO (non destructive read out) that has a transistor as a memory cell. For the NDRO-FRAM, a ferroelectric gate structure is required and then, to date, it is still difficult to obtain a good quality ferroelectric thin film on the Si surface and reduce the interface trap density between the ferroelectric thin film and the Si[3,4]. Therefore, it has been proposed to introduce an insulator into the ferroelectric thin film and the Si. In this work, we have investigated the electrical properties of $Pt\text{-}SrBi_2Ta_2O_9\text{-}CeO_2\text{-}Si$ for the Metal-Ferroelectric-Insulator-Semiconductor (MEFIS) field effect transistor.

## 2. Experimental

$CeO_2$ films are deposited on p-type (100) Si substrates by rf-sputtering of Ce target (purity = 99.99 %) in the reactive oxygen ambient. The deposition rate of $CeO_2$ film is 2.2 nm/min and the thickness of $CeO_2$ is determined with Rutherford backscattering spectroscopy (RBS). $Sr_xBi_yTa_zO_9$ (x/y/z = 0.75/2.4/2) films are prepared by metal organic deposition (MOD) method on $CeO_2/Si$ substrate and baked respectively 250°C and 400°C for 5 min. The SBT films are post annealed at 800°C for 1 hr in the oxygen atmosphere. These processes are repeated for the multi-layered structures. A top Pt electrode of 2 $x10^4$ $\mu m^2$ diameter is patterned for the MFIS capacitor and the capacitors are annealed again at 600°C for 30 min in the oxygen atmosphere. The crystallinities of $CeO_2/Si$ and $SBT/CeO_2/Si$ structures are characterized by X-ray diffraction (XRD) measurement. The I-V, C-V and the ferroelectric properties of the $Pt/SBT(200nm)/Pt/SiO_2/Si$ are measured with HP 4140B, 4284A and RT66A. The compositions of SBT films are analyzed by wavelength disperse spectrometry(WDS). The interface of the SBT/CeO/Si is observed by high resolution cross sectional transmission electron microscopy(HRX-TEM).

## 3. Results and Discussion

Figure 1 shows that the structure of the $CeO_2$ film deposited on Si at 30 °C. The $CeO_2$ has (111), (220), and (311) oriented polycrystalline phases. After annealing at 800°C for 1 hr the crystal structure does not change. The SBT films on the Pt electrode or the $CeO_2$ have a preferential orientation of (105) after the annealing at 800°C for 1 hr in oxygen atmosphere.

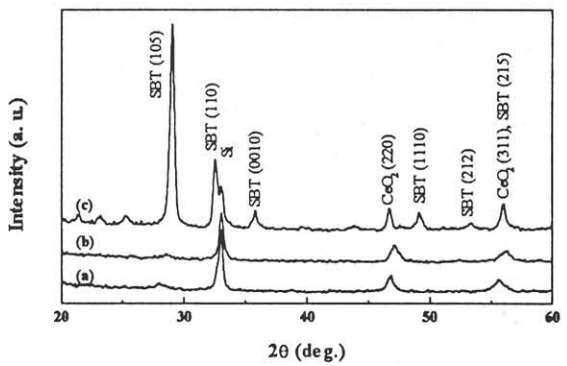


Fig. 1 XRD patterns of (a) as-deposited $CeO_2/Si$ at room temp. ,(b) annealed $CeO_2/Si$ at 800°C for 30 min., and (c) annealed $SBT/CeO_2/Si$ at 800°C for 1 hour.

The stoichiometry of the $Sr_xBi_yTa_zO_9$ (x/y/z = 0.75/2.2/2) is nearly equal to the composition of the MOD solution although the Bi component decreases from 2.4 to 2.2 due to the evaporation of Bi atoms during the annealing. The polarization characteristic of $Pt/SBT(200nm)/Pt/SiO_2/Si$ (Fig. 2) shows that the remnant polarization Pr is 9.6$\mu C/cm^2$ at 3V(150kV/cm) and increases to 11.8$\mu C/cm^2$ at 5V. The coercive field Ec is respectively 85kV/cm at 3V and 95kV/cm at 5V. A typical leakage current characteristic of SBT film is about $10^{-7}$ $A/cm^2$ at 10 V and the breakdown voltage is 4.5V(225kV/cm). The retention cycle test shows that Pr decreases about by 10% after $1x10^{10}$ cycles.

The memory window of the MEFIS ($Pt/SBT/CeO_2/Si$) structure is investigated for the application of the NDRO memory devices. The thickness of SBT films is 80, 160, and 240nm and the $CeO_2$ film is fixed at 25nm. As shown in Fig. 3 the hysteresis voltage determined from the 1MHz C-V characteristics of the MEFIS structure indicates so-called memory window of NDRO device. For the case of $Pt/SBT(160nm)/CeO_2(25nm)/Si$, according to the applied

voltage of 4, 5 and 6V, the memory window increases to 0.9, 1.4 and 2V. HR X-TEM (Fig. 4) shows that the interface of SBT/$CeO_2$/SiO2/Si is very smooth and there is no interaction although the 5 nm thick $SiO_2$ exists. Therefore, the $C_{max}$ (122pF) measured in the accumulation region is the total series capacitance of SBT, $CeO_2$ and $SiO_2$. Assuming that the relative dielectric constants of $SiO_2$, $CeO_2$, and SBT layers are each 4, 25, and 250, we can obtain the voltages divided into SBT, $CeO_2$ and $SiO_2$ layers.

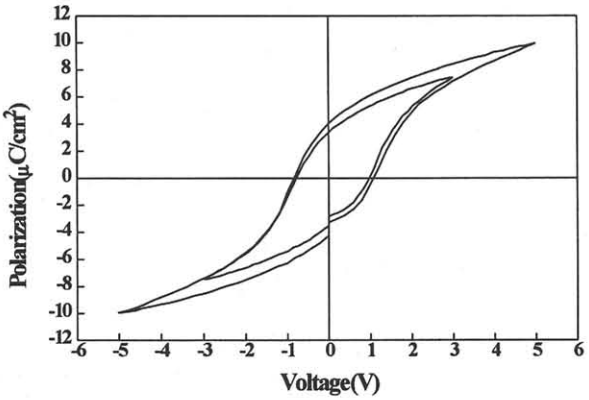


Fig . 2 P-E characteristics of Pt/SBT(200nm)/Pt/$SiO_2$/Si structure.

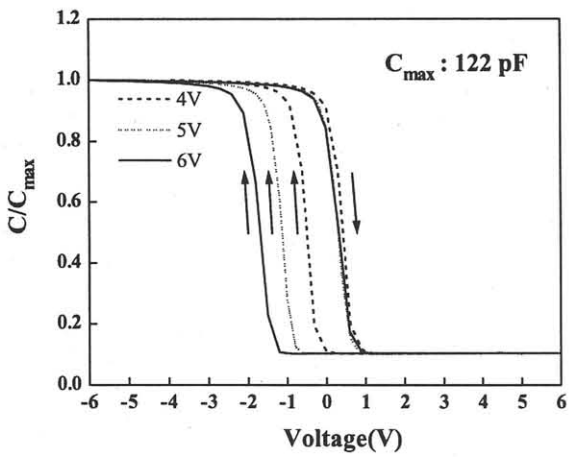


Fig. 3 C-V characteristics of SBT(160nm)/$CeO_2$(25nm)/Si structure at 1MHz.

Figure 5 shows the hysteresis voltage corresponding to the thickness of SBT films. The applied voltage of the SBT (240 nm) $V_{SBT}$ is 0.3 times the total voltage $V_T$ and $V_{SBT}$ of the SBT (160 nm) is 0.23$V_T$. But, 80nm of the SBT film has smaller memory window due to the charge injection into the $SiO_2$ because much higher electric field is applied to the $SiO_2$ layer and the smaller electric field is applied to the SBT.

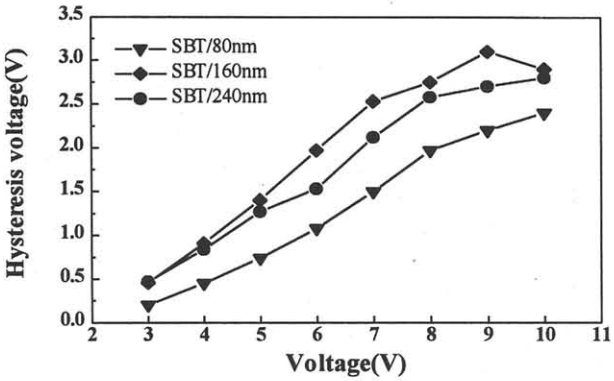


Fig. 4 Hysteresis voltages of MFIS structure of SBT/$CeO_2$(25nm)/Si with a different thickness of SBT films

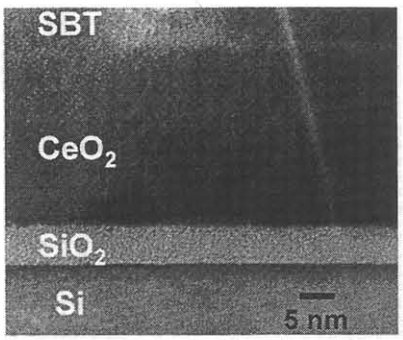


Fig. 5 Cross-sectional view of SBT(160nm)/$CeO_2$(25nm)/Si structure by high resolution TEM.

## 4. Conclusion

MEFIS (Pt-$SrBi_2Ta_2O_9$-$CeO_2$-Si) structure has been proposed for the NDRO-FRAM. The memory window of MEFIS can be controlled with the thickness ratios of the SBT/$CeO_2$: the higher thickness ratio of the SBT/$CeO_2$, the higher memory window is since the applied voltage of the SBT increases with the thicker SBT. The typical memory window of Pt-SBT(160 nm)-$CeO_2$-Si is 0.9 - 2V in the applied voltage range of 4-6V. These memory windows will satisfy the practical application of the NDRO-FRAM operating at low voltage.

### References


1) J.F. Scatt and C. A. Araujo : Science **246** (1989) 1400.
2) H. Isiwara: Jpn. J. Appl. Phys. **32** (1993) 442.
3) E. Tokumitsu, K. Itani, B.K. Moon and H. Ishiwara : Jpn. J. Appl. Phys. **34** (1995) 5202
4) Y. Tarui : 1994 IEEE Int. Electron Devices Meet.(IEEE, New York, 1994) **1**. 2.