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Electron Charging to Silicon Quantum Dots as a Floating Gate in MOS Capacitors

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Capacitance-voltage characteristics of n^+ poly-Si gate MOS capacitors with self-assembled silicon quantum dots as a floating gate have shown a unique hysteresis associated with electron charging or discharging to the Si dots by direct tunneling through a 3.5nm-thick bottom oxide. From the steady state analysis of C-V characteristics it is found that approximately one electron per dot is stably retained around zero gate bias, showing the memory effect by the Si quantum dot floating gate.

1. Introduction

MOS memories with a silicon nanocrystal floating gate is attractive because of multivalued charging of electrons[1, 2]. Recently self-assembled silicon quantum dots have been fabricated on SiO_2 by LPCVD, and the resonant tunneling through SiO_2/a single Si quantum dot/SiO_2 double barrier structures has been demonstrated at room temperature[3].

In this paper, MOS capacitors with self-assembled Si quantum dots as a floating gate have been fabricated and the electron charging to the Si dots has been evaluated from the flat-band voltage shift and the surface potential analysis of the capacitance-voltage characteristics. The memory effect by Si quantum dot charging is demonstrated.

2. Experimental

The structure of a MOS capacitor with Si quantum dots as a floating gate is schematically shown in Fig.1. Single-crystalline Si quantum dots were first self-assembled by LPCVD of pure SiH_4 at 580℃ on 3.5nm-thick SiO_2 thermally grown on p-Si(100). To increase the number of Si dots, the second LPCVD was carried out under the same conditions after surface oxidation of the first-layer Si dot array. The total dot density was ~5×10^{11} cm^{-2} as measured by AFM. The average height and diameter of as-grown Si-dots were evaluated to be 5 and 10nm, respectively. The 2nd Si dot layer surface was covered by ~1nm-thick native oxide. Subsequently, a 3.3nm-thick amorphous Si layer was grown on the Si quantum dots by LPCVD at 440℃ and fully oxidized in dry O_2 at 1000℃ to cover the Si-dots with a 7.5nm-thick oxide layer. No significant change in the surface morphology was observed in this oxide layer fabrication. Finally, 300nm-thick n^+ poly-Si gates were grown. The capacitance-voltage characteristics of the MOS capacitors with a gate area of $2.5\times10^{-3}cm^2$ were measured in the frequency range 1-100kHz at room temperature.

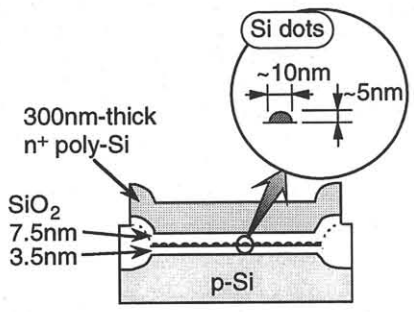

Fig.1 The Schematic cross-sectional view of MOS capacitor with Si dots embedded in the gate oxide.

3. Results and Discussion

The measured C-V characteristics of a floating gate MOS capacitor are shown in Fig.2 for different sweep rates of 19-134mV/s. The unique hystereses shown in the figure were well reproducible and almost independent of the measured frequency range of 1-100 kHz. This C-V characteristics can be interpreted in terms of electron charging and discharging to the Si dots by direct electron tunneling from the Si substrate to the dot through a 3.5nm-thick bottom oxide. Since no electron exists in the dots after applying a gate bias of -4V, the accumulation capacitance agrees well with the calculated one in which the Si dot array is regarded as a 10nm-thick Si layer, and the gate bias scan from -4 to 6V reproduces the calculated curve. On the other hand, as the gate voltage is reduced from 6 to 3.2V or from 0.5 to -0.8V, the capacitance increases parallel to the initial curve with a flat-band shift of ΔV_{FB1}=3.2V and ΔV_{FB2}=0.7V, respectively, independent of the sweep rate. ΔV_{FB1} and ΔV_{FB2} correspond to the dot potential increase of 2.1 and 0.45V, respectively. This indicates that the average number of electrons in a single dot are about 2.8 for ΔV_{FB1} and 1.2 for ΔV_{FB2} since the dot capacitance is about 3×10^{-19}F. By voltage scan from 3.2 to 1V, the capacitance remains constant, indicating that the flat-band voltage shift continuously occurs due to electron escape from the dots. Further, at gate biases lower than -1V, the C-V curves coincide with the initial curve due to complete discharging of the dots.

The hysteresis characteristics were measured in various voltage scan cycles as shown in Fig.3. The capacitance curve from ① or ⑥ to ② has not been affected by the voltage scan cycles. The curves of ④-⑤, ⑥-⑦ or ⑦-⑧ are all parallel to the curve ③-④ with a corresponding flat-band shift of 0.5, 0.8 and 1.8V. This suggests that the charge stored in the dots is constant around 0V and continuously changes in the capacitance plateau region ⑤-⑧.

Temporal change in the capacitance at a gate voltage of 3 or 0.2V is shown in Fig.4. At 3V, the capacitance after charging at 6V and that after discharging at -4V reach the same final state in 50 and 300s, respectively. While, at 0.2V, the two states are preserved longer than 10^3 seconds, showing a stable retention of about one electron per Si dot.

The surface potential of the Si substrate was obtained as

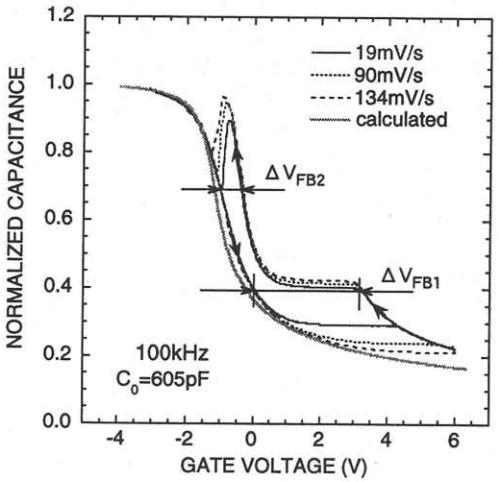

Fig.2 C-V characteristics at different sweep rates for a MOS capacitor with a Si dot floating gate. The measured curves show hysteresis due to the electron charging to the dots. The curve calculated for a MOS structure with an uncharged 10nm-thick Si floating gate is also shown as a reference.

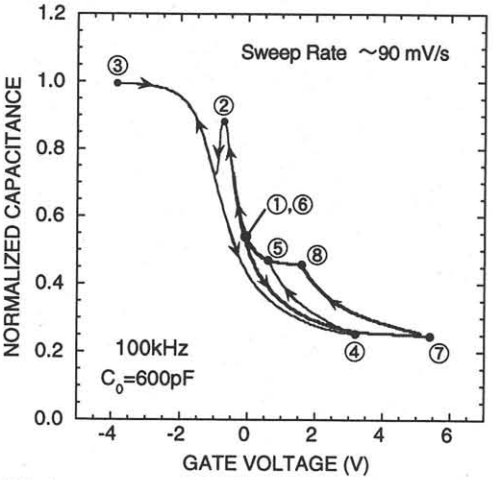

Fig.3 C-V characteristics for variety of gate bias scan. The curves of ④-⑤, ⑥-⑦ or ⑦-⑧ are parallel to the curve ③-④ with a corresponding shift of 0.5, 0.8 and 1.8V.

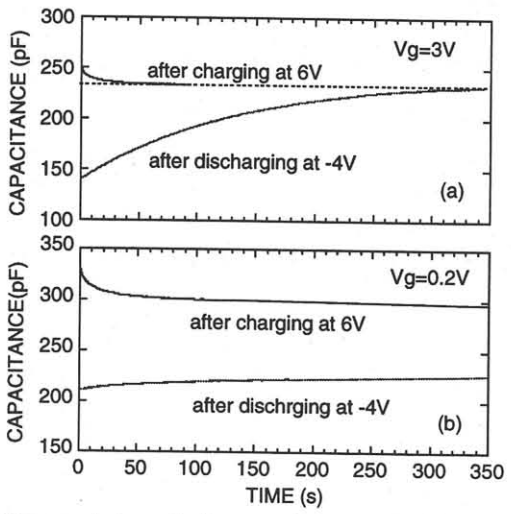

Fig.4 Temporal charge in the capacitance at gate biases of 3V(a) and 0.2V(b) after charging and discharging of Si dots.

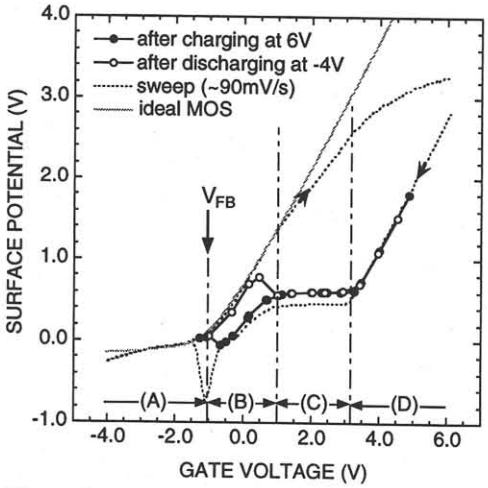

Fig.5 The surface potential of the Si substrate. The dot charging state can be divided into four regions (A)-(D).

shown in Fig.5. The dot charging level can be divided into the four regions (A)-(D). When the gate bias is lower than the flat-band voltage of -1V, no electron exists in the dots. In the (B) and (D) regions, the change in the surface potential is parallel to the ideal MOS capacitor. This result verifies the charge stored in the dots is kept constant in these region. The decrease of the surface potential of about 0.35V by electron charging in the (B) region is consistent with the fact that the dot potential increase is 0.45V because the oxide voltage in the bottom oxide is 0.1V as obtained from the total charge in the dot layer. Thus it is confirmed that approximately one electron is stored in a single quantum dot in the (B) region. Further, the surface potential of 0.6V is maintained at gate voltages in the region (C), indicating continuous decrease in electron number per dot with decreasing gate bias.

4. Conclusions

The electron charging to the Si quantum dots as a floating gate of MOS capacitors was evaluated. It is shown that the dot charged state can be divided into the four regions depending on the gate bias. It is also found that around zero gate bias nearly one electron is retained in a single dot and the maximum number of charged electrons in a single dot is three at gate voltages ranging from 3.2 to 6V.

Acknowledgments

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