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Suppression of Unintentional Formation of Parasitic Si Islands on a Si Single-Electron Transistor by the Use of SiN Masked Oxidation

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1. Introduction

Recently, Si single-electron tunneling structures have been attracting much attention from the viewpoint of their application to practical electronic devices. One possible way to fabricate such devices is to utilize Si islands naturally formed due to structural randomness. There have been several reports on the operation of single-electron transistors (SETs), which results from the unintentional formation of Si islands due to structural fluctuation in wires [1] or even in two-dimensional (2D) layers [2]. Though this kind of method easily provides multi-island structures, the controllability for the formation and arrangement of the islands is poor.

As a method with good controllability, we have reported so far that pattern-dependent oxidation [3,4] in Silicon-on-Insulator (SOI) substrate can produce a high-temperature operating SET [3] or a single-electron memory [4] by the self-aligned formation of Si islands. Figure 1(a) shows a schematic diagram of our SET. Thermal oxidation converts a Si wire into a single Si island by forming tunnel barriers at each end of the wire [3]. Because the thermal oxidation of Si is a very stable process, the technique has good reproducibility. However, unintentional formation of Si islands can also take place in some cases. Since the poly-Si gate covers the pad Si layers as well as the SET island, parasitic n-channel MOSFETs are formed on both sides of the SET as shown in Fig. 1(b). When the 2D Si layer of the MOSFETs is extremely thin, multi-island structures may form there.

In this paper, we investigate the problem of parasitic islands, which is often faced in the Si/SiO_2 system. We show a way to identify the electrical characteristics of the parasitic islands, which may screen those of an island formed by design. Moreover, we propose a fabrication technique by which the unintentional formation of parasitic islands can be suppressed.

2. Backgate voltage dependence

In this section, we show that the backgate (substrate) voltage (V_b) can be used to distinguish the electrical characteristics of the intrinsic island from those of the parasitic islands. This becomes possible because the V_b dependence differs a lot between the two types of the islands. Figure 2 shows the source-drain current (I) as a function of the gate voltage (V_g) for various V_b's. Figure 2(a) shows typical characteristics of the intrinsic Si island for a device with relatively thick Si. The periodic oscillation indicates the formation of a single island. The ratio of peak shift ΔV_g to increment ΔV_b is 0.01. On the other hand, $\Delta V_g/\Delta V_b$ is much larger for the parasitic islands. Figure 2(b) shows the case for another device with thinner Si. The ratio $\Delta V_g/\Delta V_b$ is as large as 0.11. The oscillation is due to multi-island structures, which are naturally formed in a thin Si layer of the parasitic MOSFETs. The characteristics due to the intrinsic island are completely concealed.

The big difference in $\Delta V_g/\Delta V_b$ is explained as follows. The ratio $\Delta V_g/\Delta V_b$ is equivalent to the ratio C_b/C_g, the ratio of the backgate capacitance to the front gate one, as shown in Fig. 1(b). In the case of the intrinsic island, it is considerably small because of the geometrical structure of the island and the covering front gate. Figure 3 shows a cross-sectional TEM image of a Si wire and its schematic diagram. Since the Si wire is almost completely surrounded by the poly-Si gate, most of the electric fluxes into the wire come from the front gate and only part of them come from the backgate across the buried SiO_2. In contrast, C_b/C_g is relatively large for the parasitic islands since they exist in the 2D Si layer of the MOSFETs. The value becomes close to the thickness ratio of the gate oxide (70 nm) to buried oxide (400 nm) because the situation is similar to that of parallel electrode-plates. Thus, we can identify the I-V_g

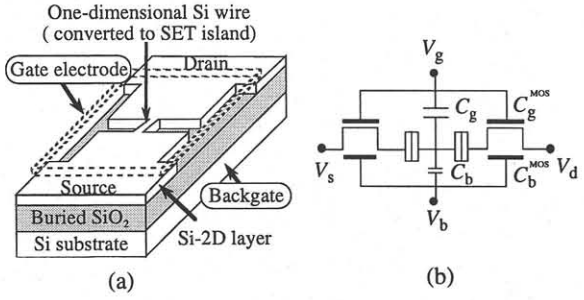

Fig. 1 (a) Schematic diagram of a Si SET. (b) The equivalent circuit.

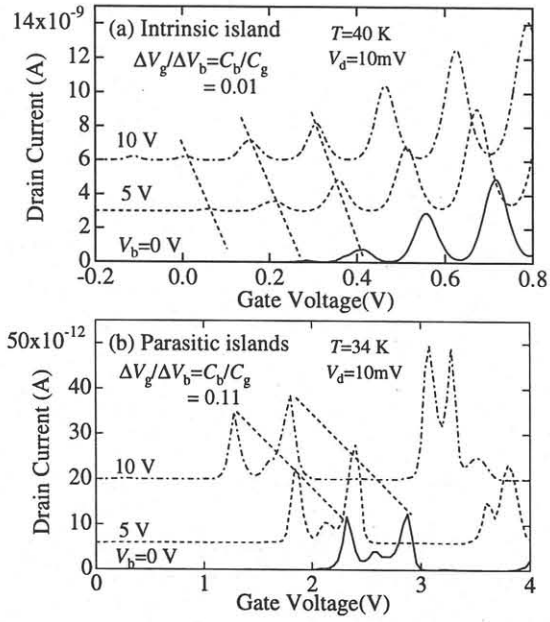

Fig. 2 I-V_g characteristics for (a) Si-SET with a relatively thick Si layer and (b) another SET with a thin Si layer. The curves are vertically offset for clarity. Note the different voltage scales for (a) and (b).

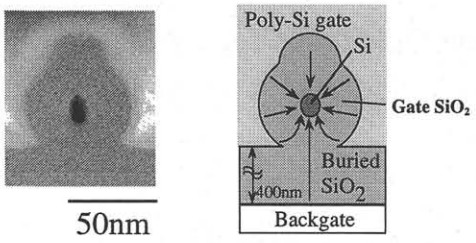

Fig. 3 Cross-sectional TEM of the Si wire and its schematic diagram.

characteristics of the parasitic islands by examining $\Delta V_g/\Delta V_b$.

It should be added that the selective gate-control is also useful for investigating the intrinsic island as shown in Fig. 2(a). Because the Si layer is relatively thick, the parasitic MOSFETs do not affect the characteristics seriously. However, one can see that new current peaks appear in the low V_g regime with increasing V_b. These peaks are suppressed when V_b is zero because the channels of the parasitic MOSFETs are closed in the low V_g regime. Thus, parasitic resistance of MOSFETs often conceals the peaks in the so-called "few-electron regime", where the number of electrons in the Si island is small. Such a regime can be revealed and investigated by applying a positively high V_b [5] because it can selectively shift the threshold V_g of the parasitic MOSFETs in the negative direction, while it does not shift the characteristics of the intrinsic island so much.

3. SiN-masked pattern-dependent oxidation

Here we propose a fabrication technique that can prevent the unintentional formation of parasitic islands. The key process is the use of a stacked structure of SiO_2 (28-nm thick) and SiN (22-nm thick) layers in the pattern-dependent oxidation as shown in Fig. 4. The surface SiN layer prevents the unnecessary thinning of the Si pad layer because it retards oxygen diffusion from the surface side. On the other hand, the essential processes for the formation of the intrinsic island are maintained; the enhancement of oxidation near the pattern edge and the suppression of oxidation in the wire due to stress built-up [3]. Because we use a SiO_2 layer beneath, whose thickness is similar to the width of the Si wire, the oxidation in the pattern-edge proceeds to the same extent as the case without the SiN layer, and so does the oxidation in the wire. Figure 5 shows the I-V_g characteristics for fabricated devices. The result at 43 K for the device with relatively thick Si is shown in Fig. 5(a). A clear

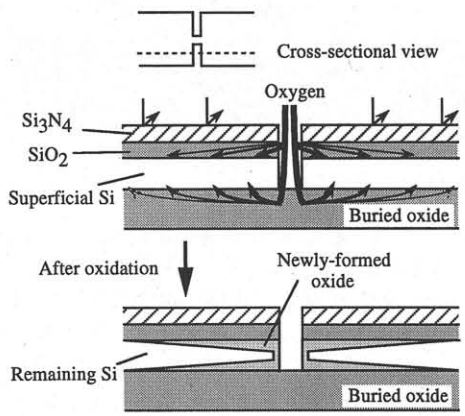

Fig. 4 Schematic diagram of SiN-masked pattern-dependent oxidation. The Si layer away from the pattern-edge remains thick.

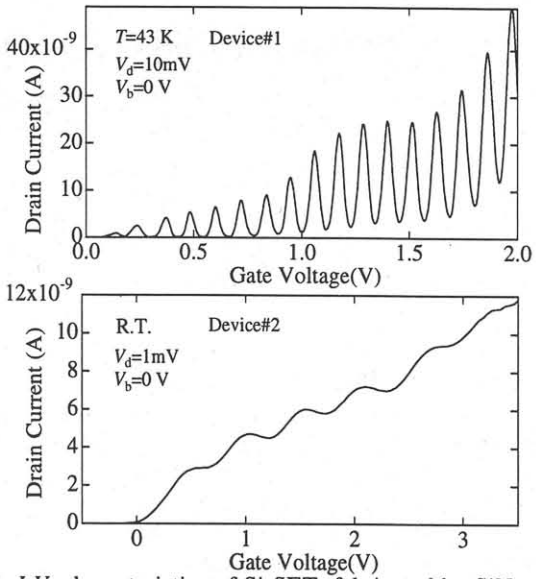

Fig. 5 I-V_g characteristics of Si-SETs fabricated by SiN-masked pattern-dependent oxidation. (a) The device with relatively thick Si and (b) the other device with a thin Si layer.

and periodic oscillation is observed. What is most striking is the case for another device with a thinner Si layer. Figure 5(b) shows the characteristics for the device whose intrinsic island thickness is almost the same as that of the device in Fig. 2(b). A distinct and periodic oscillation is observed even at room temperature. This indicates that the formation of the parasitic islands is effectively suppressed by SiN-masked pattern-dependent oxidation. We believe this kind of local oxidation technique is a promising process for fabricating single-electron devices on SOI substrates.

4. Conclusion

Even defined lithographically, Si-SET structures in the ultrathin Si of SOI substrates are often accompanied by accidentally formed parasitic Si islands. This situation becomes aggravated as the size of the intrinsic island is reduced. We have shown that this problem can be surmounted by the use of a SiN mask layer for the pattern-oxidation process. Moreover, it has been shown that the backgate is useful for distinguishing the electrical characteristics of the intrinsic SET island from those of the parasitic islands.

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