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Fabrication Process of Si Memory Dot and Quantum Channel Based on As Dopant Statistical Distribution Effect

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1. Introduction

Single-electron memory , which operation is based on the storage of very few electrons (possibly one) in a memory dot embedded between a MOSFET channel and a control gate, has recently attracted much attention. This is mainly due to an emerging demand for high density and low power dissipation in future integrated circuit devices. It is very important to develop a simple process in the fabrication technology of Si single-electron memory. Up to now, there have been several reports about fabrication process of single-electron memory on Si substrates and SOI wafers [1]-[3], however, these processes utilized very fine electron-beam lithography and complicated technology. This paper purposes to develop a simple fabrication process of Si single-electron memory based on As dopant effect in accordance with the mechanism described below.

2. Theory

For the oxidation of thin nanostructure and zero initial oxide thickness, the linear oxidation law[4] is given by the following relationship:

$$\frac{Xo}{(B/A)} = t \qquad (1)$$

where Xo = oxide thickness, t = oxidation time, (B/A) [5] is linear rate constant dependent on oxidation conditions:

$$(B/A) = (B/A)^{i}[1 + K' C_{VT}^{i} e^{+0.2/KT}(C_{VT}' - 1)] \qquad (2)$$

where C_{VT}' is normalized total vacancy concentration ($V^{+}, V^{-}, V^{=}$ included), and other quantities are defined as in Ref. [5].

It was reported that the Si oxidation rate can be enhanced by heavy doping which produces substantial increase in the oxidation linear rate constant (B/A) with increased substrate doping. The reason is that the doping level shifts the position of Fermi level, which results in enhanced vacancy concentration C_{VT}'. These point defects may provide reaction sides for the chemical reaction converting Si to SiO_2, thereby increasing oxidation rate through Eq.(1).

In nanostructure fabrication, we should take into account the dopant statistical distribution effect. When As is implanted into a Si substrate at 110 keV, its concentration reaches a peak at 50 nm from the surface and the ratio of pileup to the other position As concentration is very large. This results in significant enhancement of oxidation linear rate constant at the As peak concentration. Based on this effect, this paper demonstrate, experimentally, the possibility to perform a memory dot and a quantum wire channel simultaneously in one process .

3. Experiment and result

Our fabrication process was carried out as follows: As was implanted (at 110 keV, 1E14 cm^{-2}) into a Si wafer before deposition of a thin Si_3N_4 layer which protects the top of the Si from oxidation. Then, an etched trapezoid mesa is formed by electron-beam lithography and RIE . The height and the top width of the trapezoid mesa are 400 nm and 100 nm respectively. After the mesa being subjected to oxidation, a small silicon part is separated from the top of the triangular channel, two silicon wires are then produced at the same time. The process was completed by deposition of a polysilicon layer.

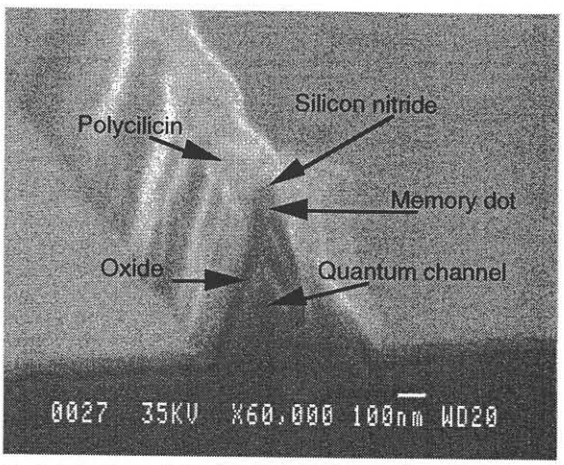

Fig.1 Cross-section of the top wire with a size of 10 nm and the 250 nm high triangular channel

Fig.1 shows a SEM image of cross-section of the sample. The light region is polysilicon and the dark one is SiO_2. The gray region is Si, where the top wire with a size of 10 nm and the triangular channel with 250 nm high separated by SiO_2 can be seen. However, if an SOI wafer (silicon layer thickness of 200 nm) is used, the etching will be stopped automatically at buried SiO_2 layer. And then with a trapezoid mesa of 200 nm, we can expect getting a reduced size for the bottom triangular channel.

4. Discussion

The advantage of this process is that it does not require very fine pattern formation technology and that a memory dot, a quantum channel, and gate oxide can be performed simultaneously in one process. This is attributed to previous As statistical distribution dopant effect. Fig.2 demonstrates the result of our experimental simulation by TSUPREM-4 [6]. In the figure, As vertical profile also is illustrated. It is clearly evidenced that the position of the maximum oxidation rate corresponds to the As peak concentration in statistical distribution, which is determined by the doping energy. This fact points out that the doping energy can be selected to realize a particular structure.

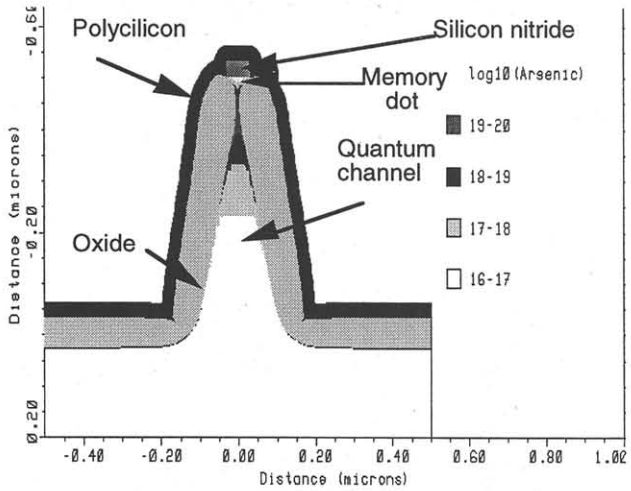

Fig.2 Cross-section of the trapezoid mesa simulated with As after oxidation.

Identical behavior should be expected for acceptor impurities such as B, but the influence of the dopant effect is significantly less than As doped at low temperature . The reason is that B doping raises only the V^+ vacancy concentration, whereas As doping raises the both V^- and $V^=$ vacancy concentration to generate a higher C'_{VT} increase. It is worth noting that this process is sensitive to temperature, because C'_{VT} is not dependent on doping level, but on oxidation temperature.

In order to confirm the fact that the formation of the dot and the channel relies on As dopant effect, rather than on the stress caused by deposition of Si_3N_4 layer. The oxidation without Si_3N_4 mask was simulated. Identical result are obtained. This implies that the fabrication process is expected to be simple.

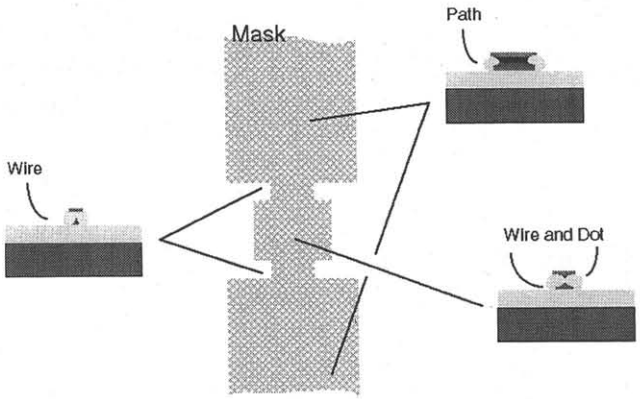

Fig.3 Mask layout for the etching of SOI silicon layer and different cross sections after oxidation of this layer. A resultant quantum memory dot device can be expected.

This technique will be used to fabricate a single-electron memory device on an SOI wafer. The layout of device is composed of a 150-by-150 nm central square and two less than 100 nm wide quantum wires which are contacted between the square and the external electrodes. It is shown in Fig.3. After oxidation, the memory dot and the channel will be performed simultaneously in the square, whereas for the others parts of layout only a channel can be made. Because the width of 150 nm is critical size. If the size is larger than it, the dot and the channel will not be separated by oxide; if the size is smaller, the dot will be oxidized completely.

5. Conclusion:

We have successfully fabricated a wire with a size of 10 nm on the top of a 250 nm high triangular channel in one process by combination making use of dopant effect and oxidation. This advanced fabrication process with a good layout choice could be used to make single electron memory device in the future.

Acknowledgments

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