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Room Temperature Nb-Based Single-Electron Transistors

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1. Introduction

Since the single-electron transistors (SETs) enable us to control individual electron one by one, the SETs have much attention as novel functional devices. In the principles of the SET, which is based on the Coulomb blockade phenomena, the size (or capacitance) of the tunnel junctions system is closely related to the operation temperature. If one could decrease the size of the junctions system further, the SETs will operate at higher temperature. From this point of view, new ultra-fine material processing techniques are necessary for the fabrication of room temperature SETs.

The scanning probe microscope (SPM)-based lithography techniques were developed using atomic force microscope (AFM) in air, which is so called AFM nano-oxidation process. The reaction mechanism on the SPM-based oxidation is considered to be an anodic oxidation, and this oxidation process proceeds through an electrochemical reaction driven by a negative bias applied to the SPM tip. Recently, we have reported that this process was successfully applied to the surface modification of Nb thin films and the modified structure was of Nb oxide [1]. In this way, one can easily obtain Nb oxide wires with feature size of ~10 nm, which suggests that lateral Nb/Nb oxide/Nb junction devices such as SETs will be realized using this fabrication process. Moreover, in order to reduce the junction size further, thermal oxidation process has been newly developed for the AFM-processed devices, in which *in situ* monitoring of the conductance variation could be possible during the thermal oxidation. In this paper, fabrication process of the Nb/Nb oxide-based SETs is described, and room temperature electrical properties are reported in detail.

2. Fabrication of Nb/Nb Oxide-Based SETs

Ultra-thin Nb films were prepared by DC magnetron sputtering technique on thermally grown SiO_2 (100 nm) layer on Si substrates. Thickness of the film was set at about 2~3 nm. Surface roughness of the film was measured by AFM and was found to be ~0.5 nm, which is smooth enough for this surface-sensitive oxidation process. To fabricate devices, Nb metal patterns were first defined by optical lithography. Each metal pattern consisted of a cross structure with the width of typically 2 μm, which is connected to large contact pads with the area of about 100 μm^2. And then the sample was mounted in a modified AFM system in which the precise control of the bias conditions for the anodic oxidation can be possible. For the AFM oxidation step, Si_3N_4 cantilevers coated with metals such as Au, Ti and Pt were used. Through the experiments, ambient humidity was not exactly controlled but was roughly kept at around 30 %.

In the AFM oxidation, entire thickness of the Nb film (2~3 nm) could be oxidized with the applied tip bias of -2 V~ -5 V. Nb oxide wires could be formed by moving the tip during the anodic oxidation. If the bias is increased negatively, the size of the wires will become larger. By adjusting the oxidation parameters such as applied bias, scanning speed and ambient humidity, the width of the Nb oxide wires could be precisely controlled from ~10 nm to >500 nm.

The fabrication step of the side-gate SET structure is as follows. First, an ultra-narrow Nb metal wire, which acts as the channel, is defined at the center of the cross structure. The channel is connected to the source and drain electrodes, by fabricating the large Nb oxide region to suppress the leak current from other electrodes. Then, tunnel barriers are formed across the ultra-narrow channel. Finally, the gate electrode is defined at the one side of the channel. Figure 1 shows the typical AFM image of the side-gate SET. In this image, the vertical color image ranges 8 nm from black to white. Nb oxide region is shown as white and Nb metal region is as black. Source, drain and gate are placed in-plane as shown in the figure, and are connected to the contact pads.

After fabricating the side-gate SETs with double junction structure, the thermal oxidation process was performed in a probe chamber in which the oxidation temperature is set at 180 °C under the controlled 20~25 % ambient humidity.

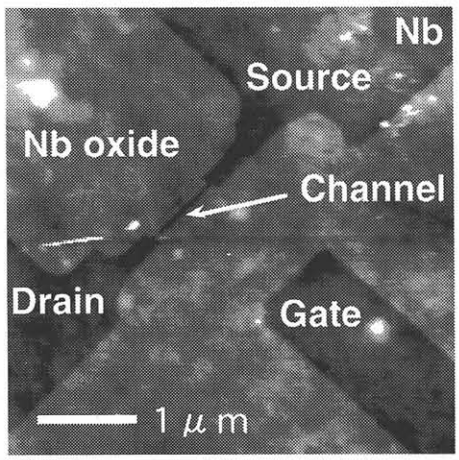

Figure 1. AFM image of side-gate SET. Tunnel junctions are not well resolved in this magnitude.

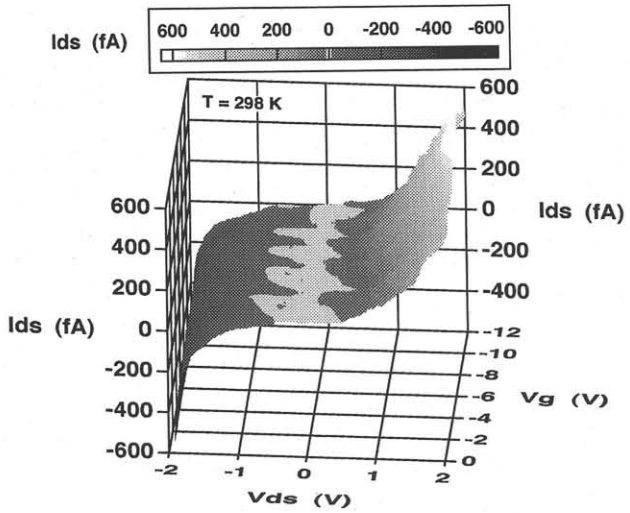

Figure 2. Drain current-drain voltage characteristics with various side-gate voltages at room temperature (T = 298 K). Drain current with ± 2 fA is colored as white.

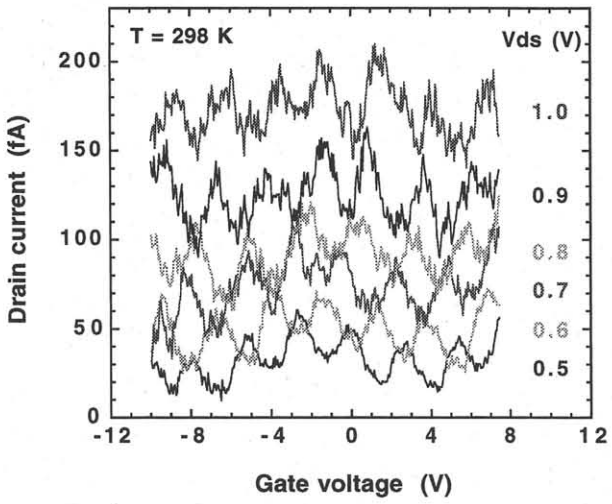

Figure 3. Drain current-gate voltage characteristics with various drain voltages at room temperature (T = 298 K).

During the thermal oxidation, the channel current was *in-situ* monitored with applying the source-drain voltage of 0.1 V in order to control the channel conductance of the device. As expected, the channel conductance G(t) was decreased with increasing the oxidizing time, and expressed as $G(t) = A - B\sqrt{t} + C \cdot t$ (t = oxidizing time, A, B and C = constant). This implies that the oxidation reaction is dominated by the diffusion limited reaction, *i.e.*, the oxide growth becomes proportional to the square root of the oxidizing time. Under this contribution, the channel conductance of the device could be effectively reduced by $<1/10^{2\sim3}$ from the initial value.

3. Electrical Properties at Room Temperature

Current-voltage characteristics of the devices were measured under asymmetric bias condition using HP4156A. Electrical measurements were performed in a shield room in which environmental temperature and humidity is controlled. Drain current-drain voltage characteristics were measured with various gate voltages at room temperature (T = 298 K) and are shown in Fig. 2. In this figure, drain current region with nearly zero level (± 2 fA) is colored as white in order to make the Coulomb blockade region clear. From this, although the current level through the device is extremely low due to the reduction of the junction size by the thermal oxidation process, the Coulomb blockade region corresponding to a charging energy of ~1 eV is confirmed and the Coulomb blockade voltage is well modulated periodically by changing the gate voltage. Furthermore, the drain current grows exponentially at higher drain voltages. This is due to the fact that the barrier suppression is caused by the image charge potential [2,3], which is well known as Schottky effect [4]. Coulomb blockade oscillation characteristics were also measured at room temperature. Figure 3 shows the drain current-gate voltage characteristics with various drain voltages. The figure is plotted without offset. As one can see, the Coulomb blockade oscillation characteristics could be observed clearly. Even at room temperature, the drain current-gate voltage characteristics are periodic and have no large background current depending on the gate voltages.

Since the thermal oxidation process was applied to reduce the size of the junction on the devices, finished structural parameters of each junction could not be resolved with observing the device surface by AFM. Therefore, in order to explain these features, junction parameters were estimated by fitting the current-voltage characteristics with the orthodox theory using the Monte Carlo method [5]. From this consideration, the experimental results were well reproduced when C_1 = 0.08 aF, C_2 = 0.05 aF, C_G = 0.06 aF, R_1 = 20×10^{11} Ω and R_2 = 30×10^{11} Ω. These results clearly suggest that in the device fabrication step the size of the junction is effectively reduced by combining the thermal oxidation process with the AFM nano-oxidation process, and higher temperature operations become possible.

4. Conclusions

Room temperature operation of Nb/Nb oxide-based SETs was successfully achieved and reported in detail. The devices were fabricated by SPM-based oxidation technique, and then the junction area was reduced by thermal oxidation. Ultra-small tunnel junctions were easily obtained by utilizing these oxidation processes, and single-electron charging effects were clearly observed through the Nb/Nb oxide-based SETs at room temperature.

References

1) J. Shirakashi, M. Ishii, K. Matsumoto, N. Miura and M. Konagai: Jpn. J. Appl. Phys. **35** (1996) L1524.
2) A. N. Korotkov and Yu. V. Nazarov: Physica B **173** (1991) 217.
3) A. N. Korotkov: Phys. Rev. **B49** (1994) 11508.
4) S. M. Sze: *Physics of Semiconductor Devices*, (John Wiley & Sons, 1981) p.250.
5) K. Mullen, E. Ben-Jacob, R. C. Jaklevic and Z. Schuss: Phys. Rev. **B37** (1988) 98.