Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 492-493

Single Electron Three-Valued Memory Array with Reading Circuits

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1. Introduction

Single electron devices have been expected to control electrons one by one by the Coulomb blockade effect [1]. If the number of electrons held in the node in each single electron device can be easily controlled, multiple-valued single electron circuits will be realized by making the multiple-logic correspond to the number of electrons. However, so far, this method has not been applied to realize a multiple-valued single electron device. We have recently found the method to realize a multiple-valued single electron memory device, which has a serially connected junction-capacitor-junction structure, by making multiple-logic correspond to the number of electrons [2].

In this paper, we have studied about three-valued single electron memory array circuits using this memory device by the numerical simulation based on the Monte-Carlo method. We have developed a single electron memory cell which consists of the memory device combined with a reading circuit. We have successfully demonstrated that a memory array constructed with the memory cells functions as a three-valued memory array, and that any of three logical values can be stored in a selected cell and stored data can be output through the reading circuit from a selected cell. The logic-operation behavior of the memory cell indicates that the memory array can be also used as a functional memory device which carries out the logical sum of input and stored data.

2. Memory cell

Fig.1 shows a schematic of a new memory cell constructed with a single electron memory device and a reading circuit.

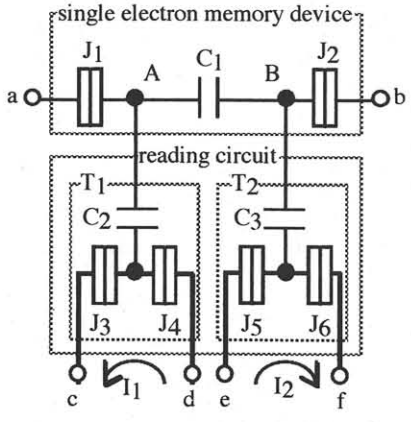

Fig.1 Schematic of a memory cell constructed with a single electron memory device and a reading circuit.

single electron memory device

The single electron memory device has one capacitor C_1 which is serially connected between two tunneling junctions J_1 and J_2. The electron configuration at nodes A and B is presented as (n_A, n_B). Since, ± charges at these nodes attract each other, the memory circuit has multiple stable states corresponding to (n_A, n_B) states. In the previous work [2], we have succeeded in operating the memory device as a three-valued memory which has three stable states of (-1, 1), (0, 0), and (1, -1). These states can be corresponded to logic "-1", "0", and "1", respectively. When we change the memory states among the three states, we apply specific voltages suitable for the changes between terminals a and b. The voltages depend on the device parameters. In this study, the capacitances and resistances of junctions J_1, J_2, J_3, J_4, J_5, and J_6 are 0.75×10^{-20} F and 5 MΩ, respectively, and the capacitances of the capacitors C_1, C_2, and C_3 are 6.0×10^{-20} F, 0.3×10^{-20} F, and 0.3×10^{-20} F, respectively. These parameters are fixed such that the frequency and thermal errors [3] at room temperature are neglected. To change the memory state from "0" to "1", from "-1" to "0", from "1" to "0", or from "0" to "-1", the voltage is set to be 9.2 V, 6.6 V, -6.6 V, or -9.2 V, respectively. These values are determined on the basis of the results of the Monte-Carlo simulation for the memory cell.

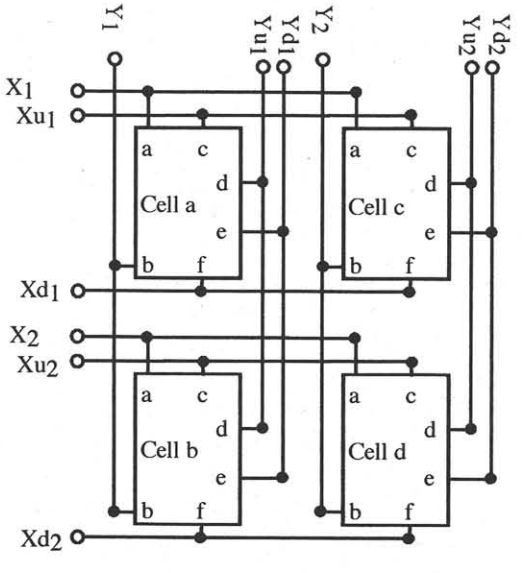

Fig. 2 Schematic of the memory array circuit constructed with the memory cells which are shown in Fig. 1.

Table 1 Three-valued operation method for the array shown in Figure 2. The cell states (-1,1), (0,0), and (1,-1) represent logic "-1", "0" and "1", respectively.

			Write(-2)	Write(-1)	HOLD	Write(+1)	Write(+2)	Read
Operation	Input signal Voltage	X_1	-4.6V	-3.3V	0V	+3.3V	+4.6V	0V
		Y_1	+4.6V	+3.3V	0V	-3.3V	-4.6V	0V
		X_2, Y_2	0V	0V	0V	0V	0V	0V
		Xu_1, Xd_1	0V	0V	0V	0V	0V	-4.6V
		Yu_1, Yd_1	0V	0V	0V	0V	0V	3.8V
		Xu_2, Xd_2, Yu_2, Yd_2	0V	0V	0V	0V	0V	3.8V
Cell State of Selected Cell a		(Initial State)						
		"+1"	"-1"	"0"	"+1"	"+1"	"+1"	"+1"
		"0"	"-1"	"0"	"0"	"0"	"+1"	"0"
		"-1"	"-1"	"-1"	"-1"	"0"	"+1"	"-1"

reading circuit

The reading circuit consists of two single electron transistors T_1 and T_2, the gates of which are connected to the nodes A and B in the single electron memory device, respectively. A stored memory state is read by measuring currents I_1 and I_2 which flow from terminal d to terminal c and from terminal f to terminal e, respectively, under the condition that the voltages at terminals a and b are 0 V. If the stored state is (0,0), $I_1 = I_2$ because the voltage at node A is equal to the voltage at node B. If the state is (1,-1), $I_1 > I_2$ because the voltage at node A is higher than the voltage at node B. In the similar manner, if the state is (-1,1), $I_1 < I_2$. Thus, the stored state is read by detecting the difference between the amounts of I_1 and I_2 currents.

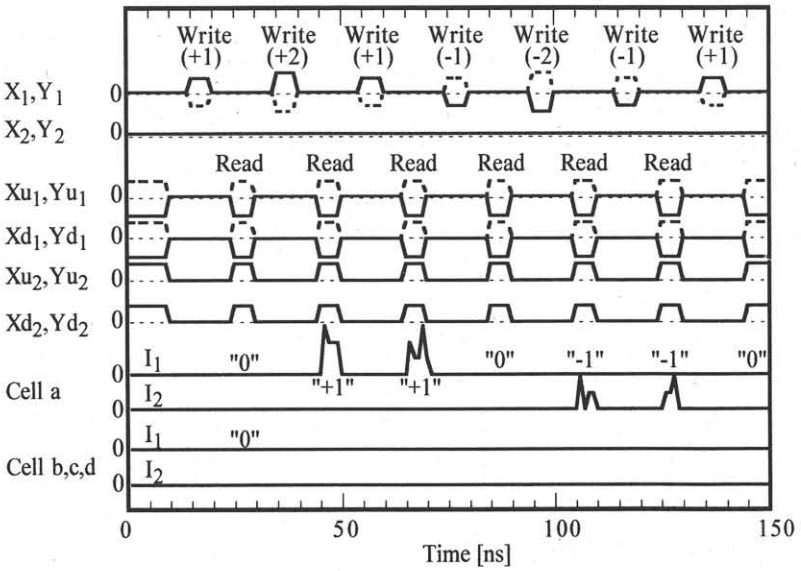

Fig. 3 Simulation of data writing and reading performances of the memory array shown in Fig. 2 under a room temperature condition. The thick lines show writing and reading voltages and data reading currents I_1 and I_2 for each memory cell.

3. Memory Array

Using this memory cell, we construct a memory array as shown in Fig. 2. When we write data in, for example, cell a, we apply the specific voltage to writing lines X_1 and Y_1 to change the cell state. When we read data from, for example, cell a, we apply the specific voltages between reading lines Xu_1 and Yu_1 and between reading lines Xd_1 and Yd_1 for reading current detection. If a cell is not selected for data reading, the same voltages are applied to the reading lines for the cell. These specific voltages are evaluated by the Monte-Carlo simulation and are tabulated in Table 1. As shown in Table 1, written data or logic is the result of a logical sum of input and stored data.

Finally, we have simulated time-dependent data writing and reading performances for the memory array using the Monte-Carlo method with the above operation conditions. The results are shown in Fig. 3. The three logical values can be read by measuring the I_1 and I_2 currents with the reading circuit. It is also confirmed that the memory logic changes in correspondence with the results shown in Table 1, and that the memory cell functions as a three-valued memory cell.

4. Conclusions

We have proposed a three-valued single electron memory array with single electron memory cells which have a serially connected junction-capacitor-junction device and a data reading circuit. Using the numerical simulation based on the Monte-Carlo method, we have demonstrated that three logical values "-1", "0", and "1" can be written and read, and that the array functions as a three-valued memory array .

Since the result of a logical sum of input and stored data can be stored in the cell, the single electron memory array is expected to function as a novel functional memory.

References

1) M. J. Kelly: *Low-Dimensional Semiconductors*, (New York, Oxford University Press, 1995) pp. 292-309.

2) K. Yamamura and Y. Suda: Proc. Si Nanoelectronics Workshop 1997, Kyoto (1997) (in press).

3) H. D. Jensen and J. M. Martinis: Phys. Rev. B**46** (1992) 13407.