Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 130-131

Invited

SOI Device Technology for Low-Voltage and High-Performance Portable Communication Systems

Alberto O. Adan, Toshio Naka, Atsushi Kagisawa

SHARP Corp., IC Group, VLSI Lab., 2613-1 Ichinomoto-cho, Tenri 632, Nara, Japan
E-mail: adan@icg.sharp.co.jp

1. Introduction

The advantages of SOI-CMOS devices over their BulkCMOS counterparts are well known [1, 2]. An attractive area for SOI is mobile wireless communication devices. The front end of portable phones operates in the RF spectrum at frequencies in the 1 to 2.5 GHz range. A key component is the frequency synthesizer PLL, which currently is mostly implemented in bipolar or BiCMOS processes due to the high speed requirements. Bipolar and BiCMOS PLL's operate at 3V, SOI opens the opportunity to reduce the supply voltage to ~1.5V, and then miniaturization. Furthermore, the full compatibility with CMOS makes possible to extend SOI-CMOS to the low frequency high density logic signal processing.

In this paper, we compare the Bulk and SOI device performance, and present a 0.35μm CMOS process for low-voltage, high performance ASIC's, implemented on ultra-thin SOI (Shallow SIMOX) wafers.

2. SOI-CMOS Device Design

CMOS devices implemented on SOI substrates demonstrate power consumption reduction of about 1/5× compared with BulkCMOS [3]. In complex LSI's, where interconnect capacitance dominates the logic gate loading, the low S/D capacitance of the SOI device is nullified. The speed advantage of the SOI logic gate is demonstrated in Fig.1, where the propagation delay of the 2-input NAND gates loaded with 0.1 pF (= 1mm metal line) are compared. Fig.2 shows the speed ratio of the BulkSi and the SOI NAND gates. Logic gates implemented in SOI substrate have a significant advantage especially at low voltage (Vdd= 1~2V). This lower operating voltage results in a major reduction in the total power dissipation, making it very attractive and efficient for high performance IC applications.

Low-voltage operation demands circuit techniques as well as low-Vth transistors. Studies of the power dissipation-speed tradeoff for operation at GHz frequency of a prescaler circuit [4] show that Vth as low as 0.25V at Vdd=1.5V is needed. It is clear that at these low Vth's, controllability and reduction of the Short-Channel Effects (SCE) are important in the SOI transistor design, as Vth variation greatly affects the OFF-state leakage (Fig.3).

The floating body and parasitic bipolar transistor action are a concern in SOIMOSFET's. These effects largely contribute to the SCE. In a Fully Depleted (FD) SOIMOSFET, the Vth lowering can be expressed as

$$\Delta Vth = \Delta\, Vth_{SCE} + \frac{S}{2.3}\cdot(1+\beta)\cdot A\cdot Vds\cdot\exp\left(-B\cdot\frac{lp}{Vds}\right)$$

where the term ΔVth_{SCE} is the normal SCE, and the last term represents the bipolar effect. S is the subthreshold swing, A, B and lp are impact ionization coefficients. From this equation follows that Vth lowering can be reduced, and controllability improved, by reduction of the parasitic bipolar current gain β.

We have applied channel-drain lateral profile engineering [5] that suppresses SCE and reduces the bipolar effect on Vth and BVdss lowering. By using this technique, implemented by a Gate Edge (GE) channel implant, excellent transistor performances and low Vth fluctuations are realized in our 0.35μm Shallow SIMOX process. Fig.4 illustrates the Vth distribution for the conventional FD SOIMOSFET and the GE FD SOI devices. The Vtsat spread is reduced by half by this channel-drain profile engineering technique.

3. Low-Voltage Device Performance

A cross-section schematic of the CMOS on SOI developed 0.35μm Shallow SIMOX process is given in Fig.5. Details of the process flow are presented in Ref.[3]. The starting substrate is a low oxygen dose SIMOX (Separation by IMplantation of Oxygen) wafer with a buried oxide layer 100 nm thick. Salicided, dual-doped polySi gates, surface channel FD CMOS transistors are realized in the 50 nm thick superficial top silicon film. A 7 nm N_2O oxide process is introduced for the gate dielectric. This process incorporates analog capacitors and resistors. These process modules increase the technology flexibility for ASIC's applications.

Logic devices and a high speed PLL circuit have been implemented in this technology. Fig.6 shows the propagation delay of different logic gates for the unloaded and the interconnect loaded (Lm=0.5mm, metal-1) cases. A prototype PLL operates at the maximum frequency of 1.6 GHz at 1.5V supply voltage, as illustrated in Fig.7. The power consumption is about 3.5mW at 1.5GHz, which is 1/5 to 1/10 the power dissipated by the BiCMOS PLL's. The power dissipation of a CPU core was reduced from 33mW at 3V and 22MHz for the 0.65μm BulkCMOS device to 15mW, at 1.5V and 50MHz, for the 0.35μm Shallow SIMOX implementation. These results demonstrate the performance of this SIMOX technology.

References

[1] Y.Kado, T.Ohno, Y.Sakakibara, Y.Kawai, E.Yamamoto, A.Ohtaka and T.Tsuchiya: IEEE IEDM Tech. Dig., pp. 665-668, 1994

[2] Y.Yamaguchi, A.Ishibashi, M.Shimizu, T.Nishimura, K.Tsukamoto, K.Horie and Y.Akasaka: IEEE Trans. Eelectron Devices, vol.40, no.1, pp. 179-185, 1993.

[3] S.Kaneko, T.Naka, A.O.Adan and A.Kagisawa: Proc. Of the 7th Intern. Symposium on SOI Technology and Devices, pp. 406-413, The Electrochemical Society (1996).

[4] A.O.Adan, T.Naka, S.Kaneko, D.Urabe, K.Higashi and A.Kagisawa: IEEE Intern.SOI Conf., pp.116-117, Oct.1996.

[5] A.O.Adan, S.Kaneko, T.Naka, D.Urabe, K.Higashi and A.Kagisawa: IEEE Intern.SOI Conf., pp.100-101, Oct.1996.

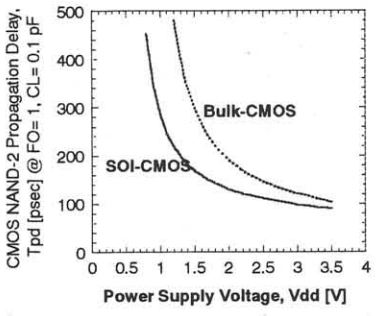

Fig.1: CMOS 2-input NAND propagation delay time comparison.

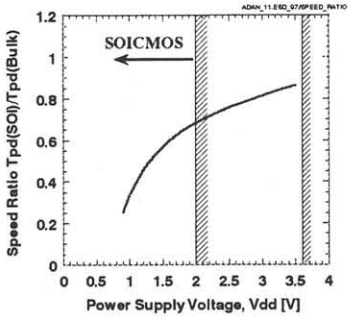

Fig.2: Speed ration of the BulkSi and the SOI NAND gates.

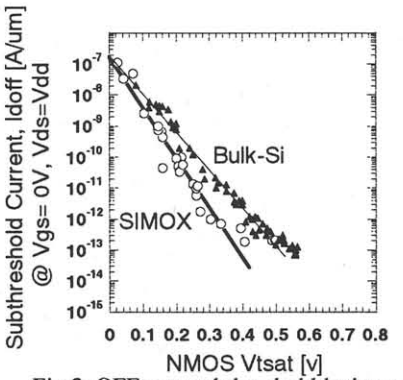

Fig.3: OFF-sate subthreshold leakage current vs Vtsat for the NMOSFETs.

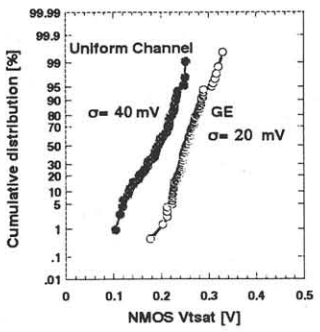

Fig.4: Vth distribution for the uniform channel and the GE SOI NMOSFET.

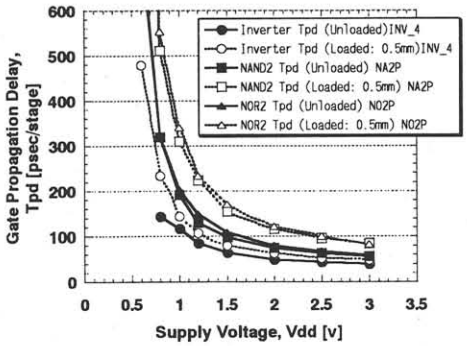

Fig.6: Propagation delay for several logic gates impalemeted in the 0.35um SIMOX/CMOS technology

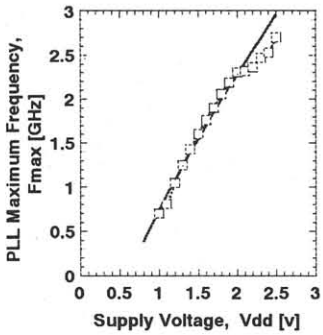

Fig.7: Maximum operating frequency for the PLL implemented in the 0.35um SIMOX/CMOS technology.

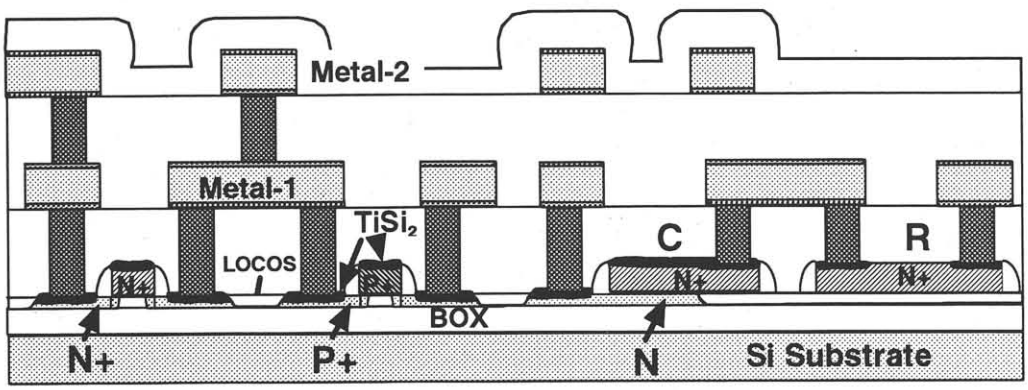

Fig.5: Cross-sectional view of the CMOS devices implemented on Shallow SIMOX substrate. A buried N-type implant is used to form the capacitor C. The resistor R is formed by avoiding salicidation on polySi layer.