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Monolithic 2 GHz and 4-6 GHz Low Noise Amplifiers Fabricated on a SIMOX Wafer

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I. INTRODUCTION

Silicon-MOS technologies for RF circuits have recently been developed in an attempt to apply an all-Si technology to L-band MMICs (Monolithic Microwave Integrated Circuits) and to their integration with digital circuits [1]. It has been pointed out that SOI technology is one candidate since compared to bulk-Si technologies it has the advantage of lower power. This advantage is enhanced at lower voltages. Although an effective way to lower the power is to reduce the supply voltage, RF performance in bulk MOS devices drastically degrades at low voltages (below 1 V). This is mainly because of increased parasitic capacitance at the drain. SOI devices, on the other hand, have excellent performance even at such low voltages. Moreover, on-chip inductors can be easily embedded in CMOS-LSIs on an SOI wafer [3]. Thus, SOI technology can be used to make low-power RF circuits with digital LSIs. Actual RF circuits on an SOI wafer, however, have not yet been reported. Therefore, we tried to make low noise amplifiers (LNA) to demonstrate the feasibility of using the SOI technology in making 2-GHz and 4-6 GHz RF circuits for the first time. In addition, we investigated extremely-low-voltage operation of these RF circuits in the low sub-1V range in order to minimize the power dissipation.

II. DEVICE FABRICATION

We used 0.25-μm CMOS/SIMOX technology for digital LSIs so that we could easily embed the RF components in the LSIs. On-chip spiral inductors had a 5-μm metal width and a 5-μm spacing and had 2-6 turns. We made low-noise amplifiers using the schematic shown in Fig. 1. We used no matching network outside. A microphotograph of the LNA is shown in Fig. 2. Results presented here were obtained with on-wafer measurements, using Cascade microwave probes, an HP8510B network analyzer, and an HP8970B noise figure meter.

III. RESULTS

For the 2-GHz LNA, the width of the nMOSFET /SIMOX was 320 μm. Finger length of the nMOSFET was 5 μm. L1-L4 of 3.2, 1.0, 5.0, 5.0 nH and C1, C2 of 1.0, 2.6 pF were used in order to matched a center frequency around 2 GHz. Self-resonance frequencies of these inductors were sufficiently high compared to the operating frequency. Figure 3 shows typical S-parameters of the 2-GHz LNA. Gain of 11.5 dB was obtained at 2 GHz and at a supply voltage of 1 V. Figure 4 shows the noise figure and the gain of the LNA as a function of frequency at a supply voltage of 1 V. The noise figure was 4.8 dB at 2 GHz and 4.2 dB at 2.4 GHz. The main contribution to this noise is from the nMOSFETs, whose noise figure measured was 3.5 dB. This rather high noise level is thought to be due to their gate resistance, because we did not use a resistance-lowering technique like silicide. Since series resistance of L2 was 4 Ω, it could not be the dominant source of the noise. Figure 5 shows S-parameters of the LNA when supply voltage was as low as 0.5 V. Even at such low voltage, the LNA gain exhibited nearly 9 dB. One application of this extremely-low voltage will be in wireless communication terminals powered by a solar cell. Since a solar cell generates 0.4-0.6 V, LSIs with RF circuits operating at such low voltages will have a big impact on the development of this kind of terminal. Figure 6 summarizes the performance of the LNA as a function of supply voltage at frequencies of 2 GHz. At 0.5 V, the gain/(power·NF) ratio was 0.72 /mW which is comparable with compound semiconductor technologies [4].

We also made a 4-6 GHz LNA whose schematic is the same as the 2-GHz one. Inductances L1-L4 were respectively 1.0, 1.0, 2.9, and 2.9 nH. Capacitors C1 and C2 were respectively 0.5 and 0.3 pF. The width of the nMOSFET/SIMOX was set at 80 μm to reduce its total capacitance. Figure 7 shows measured S-parameters of the 4-6 GHz LNA. A gain peak was observed at around 6 GHz. To the authors' knowledge, this is the first report of 4-6 GHz LNA with Silicon-MOS technology, although it has been predicted [1] as possible using deep sub-micron CMOS technology. At 6 GHz, gain, dc power, and noise figure were respectively 7.4 dB, 19.8 mW, and 7.4 dB. It is thought that the noise figure can be decreased by reducing of gate resistance. Table I is the summary of typical performance of these LNAs.

IV. CONCLUSION

We made, for the first time, 2 GHz and 4-6 GHz low-noise amplifiers on an SOI wafer using the conventional digital CMOS LSI process. The 2-GHz LNA exhibited fairly good performance during extremely-low voltage operation. At 0.5 V, the LNA had a gain/(power·NF) ratio of 0.72 /mW at 2 GHz, which is comparable with that of compound semiconductor technologies. The 4-6 GHz LNA had a gain/(power·NF) ratio of 0.05 /mW at 6 GHz. These results show that RF circuits up to 6 GHz can be implemented on SOI wafers with digital LSIs. This will have great impact on future wireless communications.

REFERENCES

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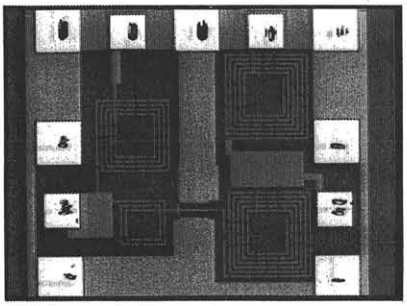

Fig. 1. Microphotograph of the low-noise amplifier. Chip size was 740 μm × 630 μm.

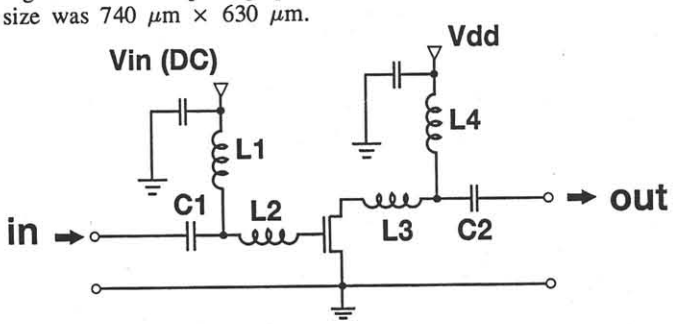

Fig. 2. Schematic of the low-noise amplifier.

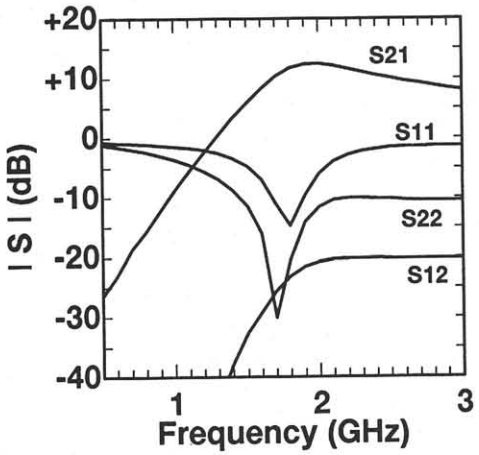

Fig. 3. Measured S-parameters of the 2-GHz low-noise amplifier at supply voltage of 1 V.

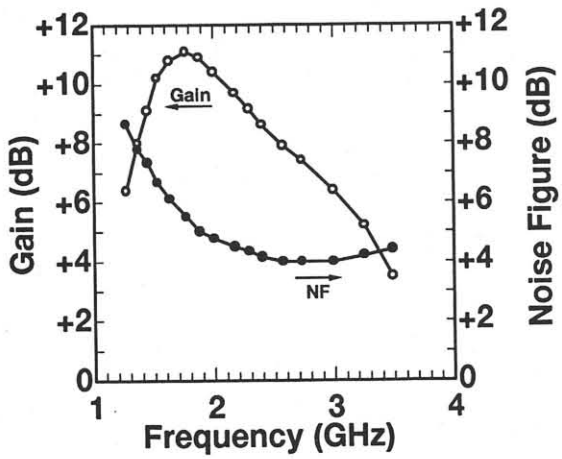

Fig. 4. Gain and noise figure of the 2-GHz low-noise amplifier as a function of frequency at a supply voltage of 1 V.

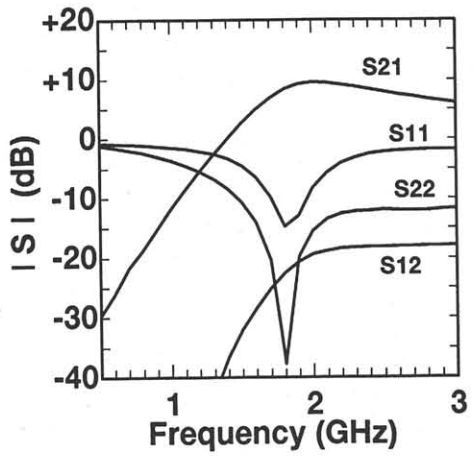

Fig. 5. Measured S-parameters of the 2-GHz low-noise amplifier at a supply voltage of 0.5 V.

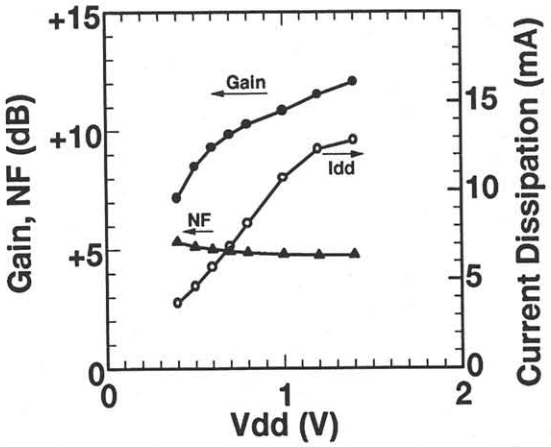

Fig. 6. Performance of the 2-GHz low-noise amplifier as a function of supply voltage at 2 GHz.

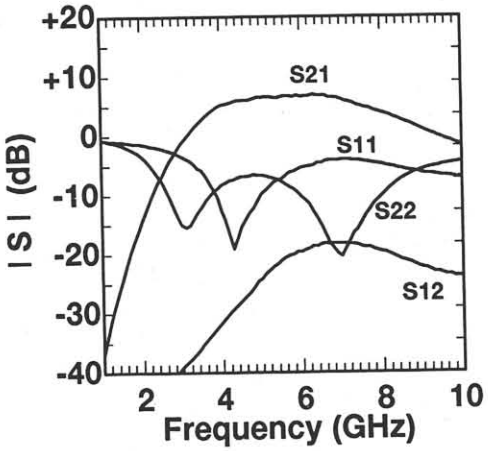

Fig. 7. Measured S-parameters of the 4-6 GHz low noise amplifier at a supply voltage of 2 V.

	2 GHz LNA	6 GHz LNA
Supply Voltage	1 V / 0.5 V	2 V
Power (DC)	10.7 mW / 2.3 mW	19.8 mW
Gain	10.9 dB / 8.5 dB	7.4 dB
NF	4.8 dB / 5.1 dB	7.4 dB
Chip Size	0.74 × 0.63 mm^2	0.74 × 0.63 mm^2

Table I. Low-noise amplifiers performance summary.