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Dynamic Data Retention Degradation in FD-SOI DRAM Cells Due to Source-Induced Charge Accumulation(SICA) Effect

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1. Introduction

SOI technology has been regarded as the promising technology for giga-bit level DRAMs due to latchup free, improved high speed and low power performance at low voltage operations, as well as simple device isolation [1]. However, serious degradation in dynamic data retention time of PD(Partially Depleted)-SOI DRAMs due to the parasitic BJT effect still remains as the bottleneck for commercialization of these devices [2-4]. For the SOI DRAMs using n+ poly gate, cell transistors suffer from transient BJT current due to partially depleted channel owing to heavily doped channel(V_{TH}~1.0V). Fig. 1 shows the threshold voltage control in SOI DRAMs using n+ & p+ poly gate materials. For the n+ poly gate transistors, heavily doped channel is required to fulfill the tight subthreshold leakage current requirement in DRAMs(V_{TH}>1.0V). Due to the absence of back-bias control(V_{BB} for bulk DRAMs), the channel doping concentration should be higher than that of conventional bulk DRAMs, and cell transistors suffer from serious dynamic data retention loss due to parasitic BJT effect(Fig. 2) and smaller current driving capability due to heavily doped channel. On the other hand, FD(Fully Depleted)-SOI transistors based on p+ poly gate provide the advantages of easier control of threshold voltages, higher carrier mobility due to low-doped channel, and reduced abnormal subthreshold characteristics. In this paper, we report transient BJT effect and dynamic data retention issues in FD-SOI DRAM cell transistors.

2. Source-Induced Charge Accumulation(SICA) Effect

Fig. 3 shows the behavior of the gate and thin film charges with respect to surface potential for FD-SOI transistor. As the source voltage V_S moves toward the positive direction, the hole quasi-Fermi level in channel is reduced by qV_S and the thin film charge curve moves along positve x-direction. The thin film charge at the operation point is determined by the cross point of gate and thin film charge curves(point A & B in Fig. 3). So, as V_S increases, thin film charge moves along A-B line and the surface potential and hole pile-up increase. So, for the FD-SOI transistor, the channel and hole distributions are strongly influenced by the source voltage. On the other hand, for the bulk MOS transistors, the hole quasi-Fermi level in the channel is pinned by the substrate bias voltage and the channel potential and the hole charge distributions are independent of the source voltage. For the bulk transistor, the channel is depleted when V_{GB} is greater than V_{FB}, and channel accumulation can be easily removed with simple bias control. But for the FD-SOI, hole begins to pile up in the channel when V_{GS}(not V_{GB}) is smaller than V_{FB}(~0.2V for p+ poly gate). Therefore, DRAM cell transistors with p+ poly gate suffer from serious hole pile-up in the thin film due to SICA effect when bit-line voltage is precharged with positive voltage(generally $1/2V_{CC}$ is used). These accumulated holes will induce BJT current when PN forward biasing is triggered by bit-line pull-down operation. Figs. 5 show the hole and potential distributions of the FD-SOI transistor for the source voltage of V_S=0.0V and 0.75V.

3. Ground-Precharged Bit-Line Sensing Scheme

In order to suppress the parasitic BJT effects in SOI DRAMs, the body-source PN junction should not be forward-biased during the active cycle operation. Recently, body refresh method combined with the boosted sensing ground(BSG) was proposed [5]. However, body refresh method has disadvantages of frequent body refresh operations and the smaller V_{CC} scaling margin due to boosted sensing ground voltage. The parasitic BJT effect can be minimized by using the ground-precharged bit-line sensing method. The ground sensing method can provide enhanced data retention characteristics and easier operation voltage scale-down capability due to elimination of the boosted ground level. Fig. 6 shows the timing diagram of the ground-precharged bit-line sensing. Fig. 7 shows the transient cell leakage current of FD-SOI with $1/2V_{CC}$ sensing, FD-SOI with ground-precharged sensing, and PD-SOI with $1/2V_{CC}$ sensing during the sequential bit-line pull-down operations. The transient BJT current of FD-SOI cell transistor is greater than that of PD-SOI cell transistor. It is mainly due to the fact that the larger amount of holes are induced in FD-SOI owing to higher V_{FB} of p+ poly gate transistor compared to that of n+ poly gate transistor. So, even for the FD-SOI transistors, the channel still suffer from hole accumulation during the precharge cycle when $1/2V_{CC}$ sensing scheme is used. It will be difficult to fully eliminate the transient BJT current in SOI DRAMs(including FD-SOI) if the bit-lines are precharged with the voltage higher than the ground voltage.

4. Conclusion

In conclusion, source induce charge accumulation (SICA) effect and its influence on the dynamic data retention of FD-SOI DRAMs are reported. The parasitic bipolar induced leakage current still remains as a critical problem for FD-SOI DRAMs if the half Vcc sensing scheme is used.

References

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[4] J. Sim, et al., IEEE ED, p. 1495, 1995.
[5] S. Tomishima, et al., Symp. VLSI Circuits, p. 198, 1996.

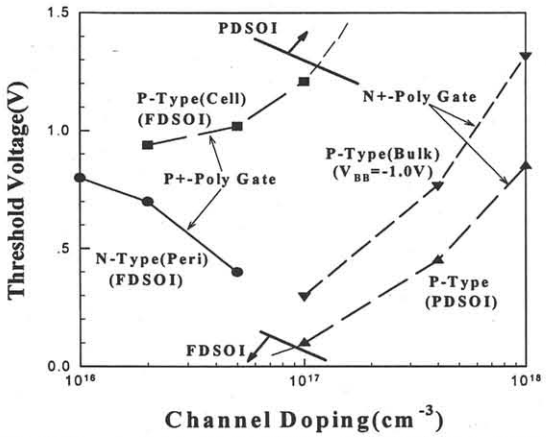


Fig. 1: V_{TH} control in SOI(toxf=70Å, tsi=1000Å, toxb=2500Å)

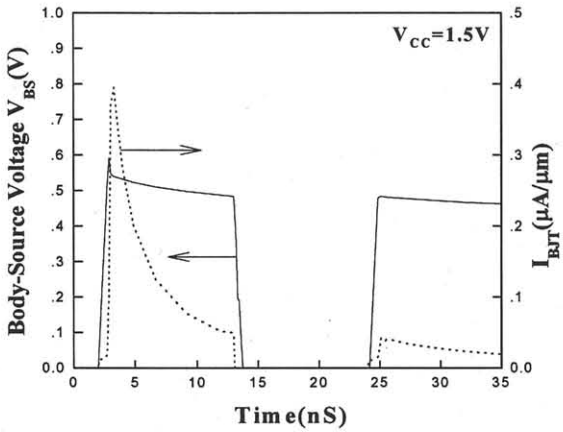


Fig. 2: Transient BJT current in PD-SOI DRAM cells during bit-line disturbs.

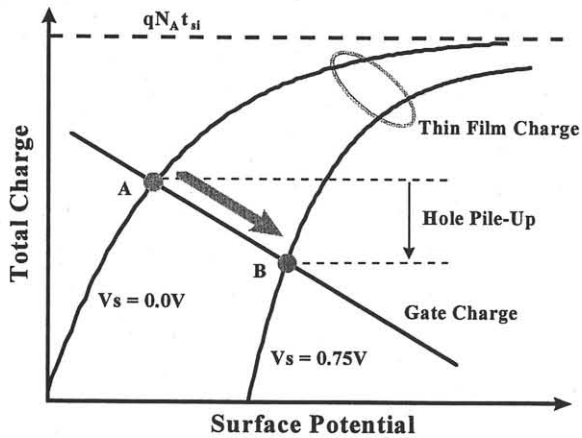


Fig. 3: Source-Induced Charge Accumulation(SICA) effect in FD-SOI DRAM Cells.

For FD-SOI DRAM Cells,

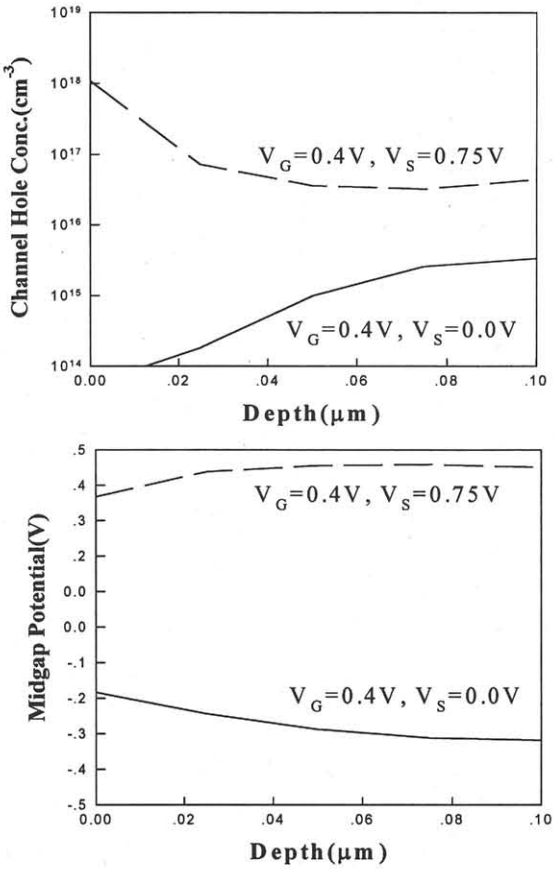
$$C_{OX}(\Psi_G - \Psi_S) = qN_A t_{si} - q\int_0^{t_{si}} p(x)dx$$

$$\cong qN_A t_{si} - q\min\{\frac{V_t}{E(0)}, t_{si}\} \times n_i e^{(-\Psi_S+V_S)/V_t}$$

For Bulk DRAM Cells,

$$C_{OX}(\Psi_G - \Psi_S) \cong qN_A x_{dep}$$

Fig. 4: Important Equations for SICA Effect.



Figs. 5: Internal channel hole & potential distributions of FD-SOI for V_S=0.0 & 0.75V.

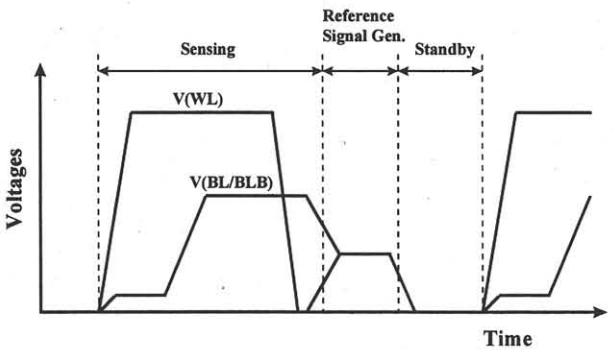


Fig. 6: Proposed Ground-Precharged Bit-Line Sensing scheme.

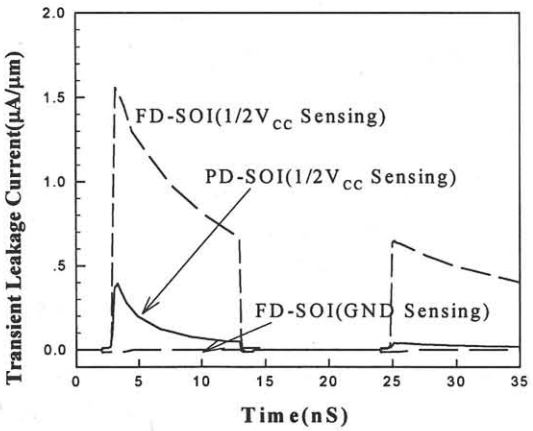


Fig. 7: Transinet BJT leakage current of FD-SOI & PD-SOI DRAM cells during bit-line disturbances.