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Simulation on A Novel Sub-0.1 μm Body Driven SOI-MOSFET (BD-SOIMOS) for Small Logic Swing Operation

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1.Introduction

SOI-MOSFET is reported to be suitable for the low voltage and low power applications[1)2)]. The advantage on the operation speed over the bulk FET is remarkable especially in the low voltage operation[1)2)]. Decreasing the applied voltage is also advantageous for a SOI-MOSFET itself, since the impact ionization, which is one of the major cause of the floating body effect, decreases. However, the hole accumulation in the floating body caused by an alpha particle incidence or by a surge pulse do not depend on the applied voltage, and it becomes a sever problem in the low voltage and low V_{th} operation, where the circuit operation is sensitive to the V_{th} variation caused by the hole accumulation. In order to solve this problem, this paper proposes a novel body-driven SOI-MOSFET (BD-SOIMOS). This device have a remarkable ability to remove holes, while keeping the drain current being comparable with the fully depleted SOI-MOSFET.

2.Device structure

Fig.1a shows the structure of n-channel BD-SOIMOS. A p^+ top-gate directly contacts with an intrinsic or an n-SOI layer (body region). The top gate is horizontally and vertically off-set from the source and drain (S/D). The n^+ S/D are located on the buried oxide. A back gate is located under the buried oxide. Typical structure parameters are shown in the table 1. The applied voltage V_{DD} is assumed to be 0.5V.

In this device, the input signal is applied to the p^+ top gate. The top gate controls the body potential, and, consequently, the drain current. The excess holes accumulated in the SOI-body are removed through the top gate. A fixed positive voltage V_{bg} is applied to the back gate, and the channel is formed in the bottom of SOI layer. The threshold voltage V_{th} can be controlled by changing V_{bg}. This characteristic is also efficient for the power management which controls V_{th}. The off-set top gate structure is adopted to weaken the electric field in the SOI layer for reducing the band-to-band tunneling current. The maximum electric field in the SOI layer does not exceed 10^6V/cm at the OFF condition. S/D located on the buried oxide is efficient for decreasing their parasitic capacitances, as in the usual SOI-MOSFET.

3.Hole exhaustion

A transient behavior of the body potential after the hole accumulation is calculated, by taking an invertor chain for an example(Fig.2a). The holes flow from the body into the top gate very fast, since this process is dominated by the drift current. The holes in the top gate node are removed through the channel of the transistor in the previous stage. Therefore, the time required to remove holes are dominated by the channel current, which is much larger than the diode current that removes the holes in the usual SOI-MOSFET. A calculation using an equivalent circuit shown in Fig.2b indicates that the holes are removed within several pico-seconds (Fig.3a). A conventional SOI-MOSFET, where the holes are removed through a diode which is composed of the source electrode and the body(Fig2c,d), requires more than 10 nano seconds (Fig.3b), since the forward bias applied to the diode is not large enough to turn on.

Table 1

Channel length L_{ch}	0.08μm
Gate length L_{gate}	0.06μm
SOI thickness T_{SOI}	10nm
Buried oxide thickness T_{BOX}	20nm
Back gate voltage V_{bg}	3.2V
Vertical off-set thickness T_{off}	5nm
Donor concentration N_D	zero (Intrinsic)

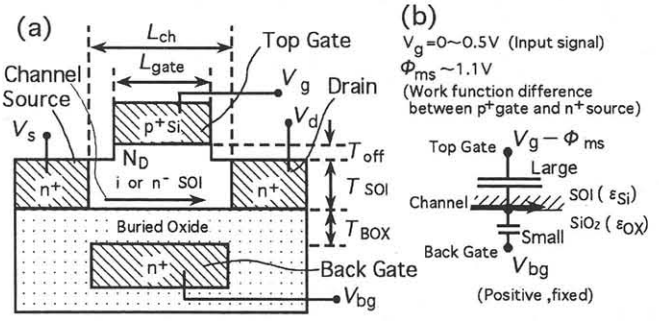

Fig.1 (a) The device structure of BD-SOIMOS.(b) The relation between the top gate and the back gate capacitance.

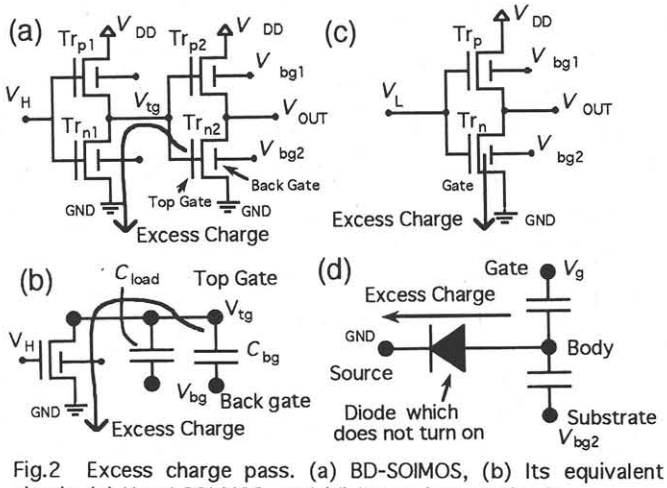

Fig.2 Excess charge pass. (a) BD-SOIMOS, (b) Its equivalent circuit, (c) Usual SOI-MOS and (d) Its equivalent circuit.

4.ON and subthreshold current

The drain current is calculated using a standard device simulator based on the drift and diffusion model. An enhancement mode operation (positive V_{th}, 0.16V), small S factor (78mV / dec.) and small V_{th} roll-off (ΔV_{th}=15mV/ ΔV_d=0.4V) are achieved (Fig.4). The diode current between S/D and the top gate at V_g=V_{DD} (<10^{12}A) is smaller than the off current at V_g=0V. The shape of the ON current curve is similar to the normal FET(Fig.5). The current value is comparable with the fully depleted SOI-MOSFET having the same input gate capacitance (Fig.6, the effective gate oxide thickness for BD-SOIMOS [T_{OXeff}] is determined from the capacitance between the top gate and the SOI back interface, where the carrier density is the highest). The off-set gate structure does not decrease the drain current, since the back gate forms the channel even in the off-set region. V_{th} can be controlled by varying V_{bg} (Fig.7).

A large top gate capacitance which is comparable with the gate capacitance of usual FET is achieved by using thin SOI layer as the body. A back gate capacitance is smaller than the top gate capacitance (Fig.1b), which is achieved by introducing the buried oxide. This relation corresponds to that for a usual FET, that the substrate capacitance is smaller than the gate capacitance. In addition, this device can enjoy the low body doping and the shallow junction determined by the SOI thickness, as in the usual SOI-MOSFET. Therefore, the device characteristics, such as the subthreshold characteristic and the ON current, are comparable with the usual SOI-MOSFET, and this device is compatible with the small logic swimg CMOS.

5.Conclusion

A body-driven SOI-MOSFET (BD-SOIMOS) is proposed. This device can remove excess holes within several pico seconds, without using additional body contact which requires additional device area. A small S factor and a small V_{th} roll-off can be obtained in the sub-0.1μm region without using very thin gate oxide.

references

1) M.Ino, et.al. Ext. Abs. ISSDM96, p.482

2) Y.Kado,et.al Tech. Dig. 1995IEDM, p.635

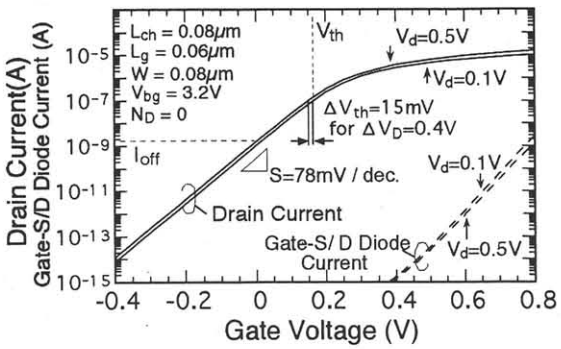

Fig.4 The subthreshold characteristics for BD-SOIMOS. The gate-S/D current corresponds to the base current of BJT. The band to band tunneling is not included in the simulation.

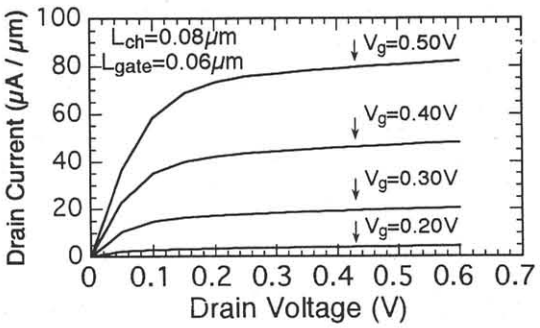

Fig.5 I_D-V_D characteristics for BD-SOIMOS.

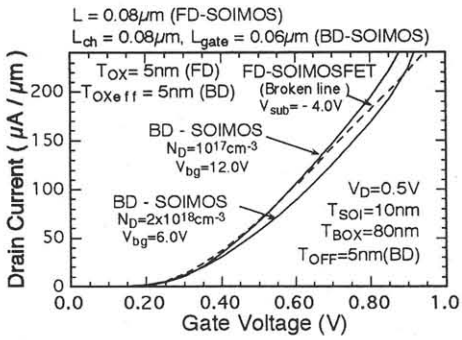

Fig.6 Comparison on the ON current at saturation region. The drain current of a BD-SOIMOS having low body concentration is comparable with the fully depleted SOI-MOSFET having the intrinsic body(broken line). The current for V_g>0.6V is increased by the lateral BJT current.

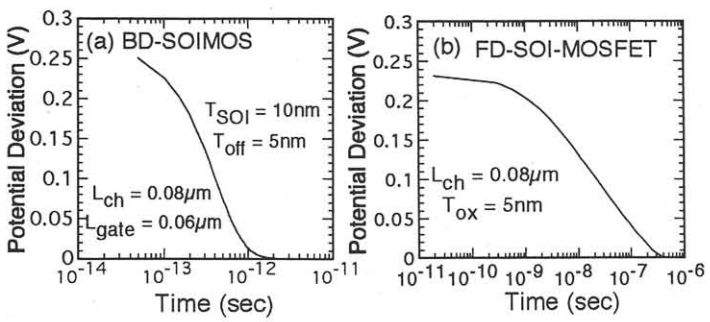

Fig3 Transient behaviors after excess holes are induced. (a) for BD-SOIMOS, (b) for a usual fully depleted SOI-MOSFET having the same channel length as (a). In (b),the potential deviation remains more than 10nsec.

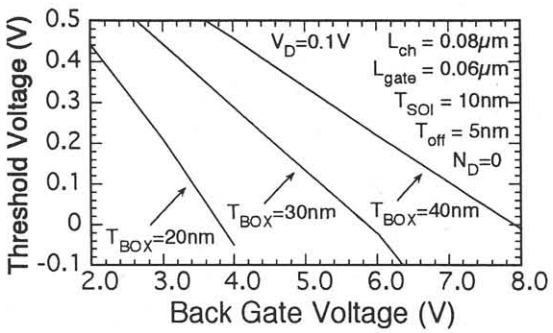

Fig.7 V_{th} dependence on V_{bg}. The result indicates that a thin T_{BOX} is suitable for decreasing V_{bg} , and that a thick T_{BOX} ,where the V_{th} weakly depends on V_{bg}, is suitable for reducing the body effect.