Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 142-143



# New Analytical Model for Subthreshold Current in Short-Channel Fully-Depleted SOI MOSFETs

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## 1. Introduction

The fully depleted SOI CMOS technology is now showing decisive advantages over the bulk technology [1]. Low-voltage (as low as 0.5 V), low-power circuits operating at high speed have been already demonstrated. To meet the requirements of high speed and low power simultaneously, the threshold voltages of SOI transistors have to be carefully determined and, therfore, accurate models for the subthreshold current in SOI MOSFET are of great importance.

## 2. New Analytical Model

A number of two-dimensional subthreshold current models have been developed recently. A two-dimensional subthreshold current models of [2], [3] are based on diffusion current equation and use a two-dimensional potential distribution, which maintains accuracy only for low drain voltage and does not reflect accurately the charge coupling between the front- and the back-gates in the fully-depleted SOI MOSFET. A model of [4] uses a number of one-dimensional approximations in the charge-sharing approach. In addition, such models use assumption of a non-constant surface potential of short-channel transistor in the lateral direction on one hand, but on the other hand use only expression for the diffusion current. A model of [5] bases its calculation on the drift-diffusion and continuity equations and analytical two-dimensional potential distribution model. However, once again the potential model used is accurate only for low drain voltage.

Therefore, we have developed a new analytical two-dimensional model for the subthreshold current of SOI MOSFET. The model takes into account both the diffusion and the drift components of the subthreshold current, the charge-sharing effect and the drain-induced barrier lowering and is based on our new analytical two-dimensional approximation of Poisson's equation solution [6], which describes the potential distribution in the SOI film using simple polynomial functions, accurately reflects the charge coupling between the front- and the back-gates in fully-depleted SOI MOSFET and yields good accuracy both for low and high drain voltage, as is shown in Fig 1 and Fig 2 for n-channel SOI MOSFET with front-gate oxide thickness 5 nm, silicon film thickness 25 nm and back-gate oxide thickness 100 nm, the doping concentration $N = 3 \times 10^{17}\ cm^{-3}$ and the channel length $L = 0.3 \mu m$.

Using the drift-diffusion current equation the subthreshold current is expressed as

$$I_D = (q\mu n_i t_{CH} W/\beta)\left[1 - \exp\left(-\beta V_D\right)\right] / \int_{l_S}^{L-l_D} \exp(-\beta\psi), \tag{1}$$

where $L$ is the channel length, $W$ is the channel width, $t_{CH}$ is the effective channel depth, $l_S$ and $l_D$ are the source-channel junction and the drain-channel junction length, respectively, and $V_D$ is the drain voltage. Analytical expressions for $t_{CH}$, $l_S$ and $l_D$ are developed using our analytical model for the potential $\psi$ and then analytical expression for the integral is obtained. In Fig. 3 a plot of $L - l_S - L_D$ versus $V_D$, calculated using our analytical model, demonstrates the channel-length modulation in weak inversion.

Model verification is provided by good agreement between the subthreshold characteristics predicted by our analytical model and the two-dimensional numerical device simulator Pisces. In Fig. 4 a Pisces-predicted subthreshold current for n-channel SOI MOSFET is compared with our analytical model for two different values of doping concentration. Since the silicon film is thin (25 nm) the dependence of the subthreshold factor on the doping concentration is weak, however relatively high doping is necessary to achieve reasonable threshold voltage. In Fig. 5 a plot of the subthreshold current versus the front-gate voltage is made for devices with varying channel length values for low drain voltage of 0.1 V, and in Fig. 6 comparison is made for high drain voltage $V_D$=2 V. Note that the threshold voltage roll-off is well-restricted and the subthreshold factor does not depend significantly on the drain voltage. Finally, in Fig. 7 a plot of the threshold voltage roll-off is shown for high and low drain voltages, where solid lines represent the analytical model and circles are Pisces simulation results. Very good agreement between the two-dimensional numerical simulations and our analytical model is observed in all plots.

## 3. Conclusion

A new two-dimensional analytical model for the subthreshold current in the fully-depleted SOI MOSFETs was developed. The model adequately describes the submicrometer devices, and, at the same time, is simple enough to be implemented in circuit simulators. It provides a very convenient tool for the design of submicron SOI MOSFETs.

# References


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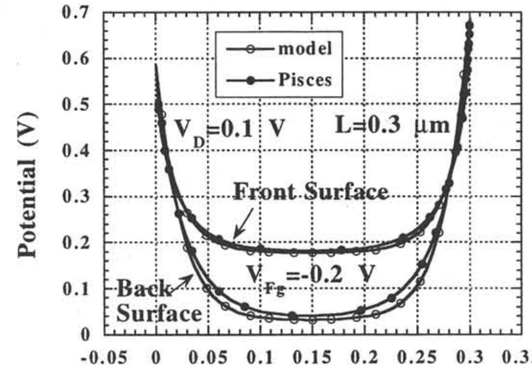


Fig 1. Plot of the front- and back-surface potentials in the silicon film for $V_D$=0.1 V

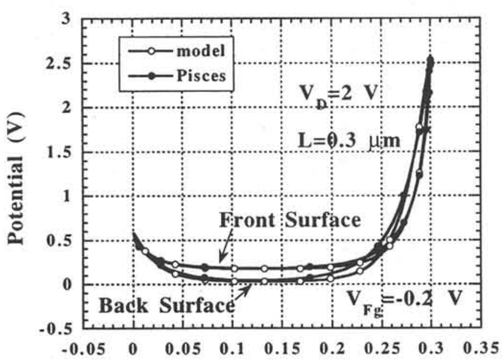


Fig 2. Plot of the front- and back-surface potentials in the silicon film for $V_D$=2 V

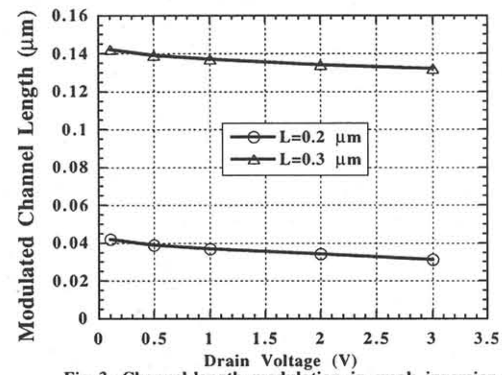


Fig 3. Channel-length modulation in weak inversion as function of the drain voltage

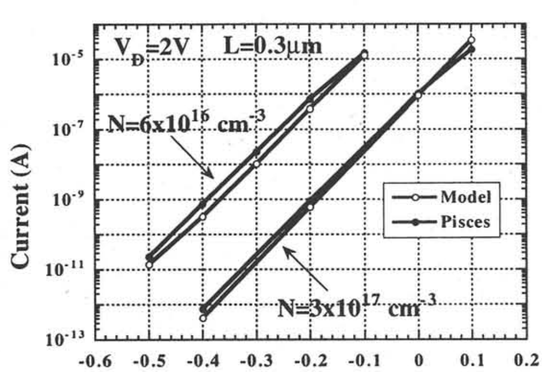


Fig 4. Comparison of model- and Pisces-predicted subthreshold current for different values of doping concentration N; L=0.3μm

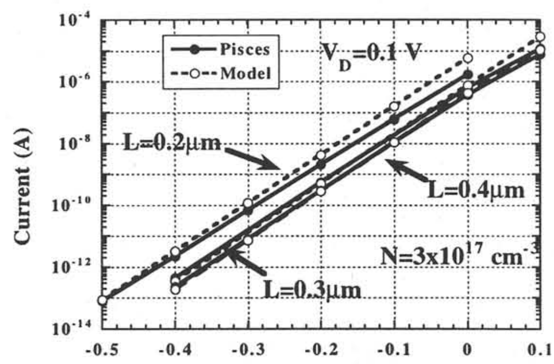


Fig 5. Plot of the subthreshold current for different channel lengths and $V_D$=0.1 V

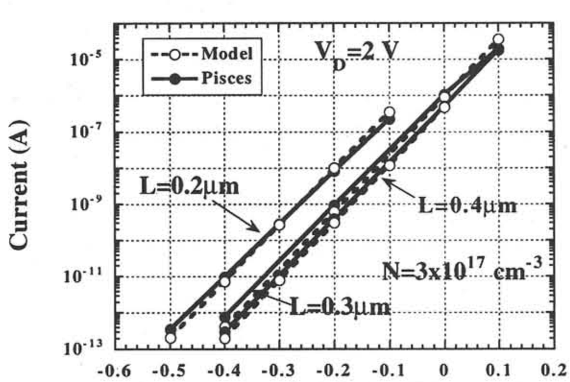


Fig 6. Comparison of model- and Pisces-predicted subthreshold current for different values of channel length; $V_D$=2V.

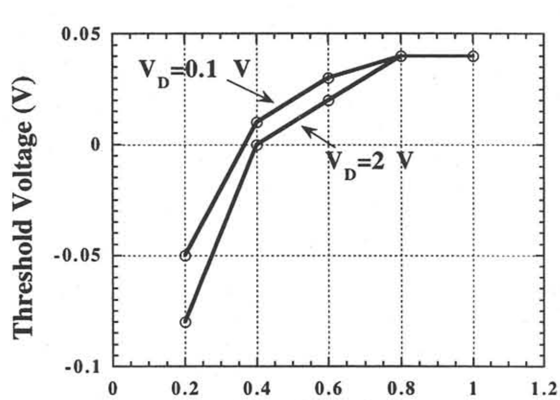


Fig 7. Threshold voltage roll-off as a function of channel length. Circles are Pisces simulation results and solid lines are analytical model calculations.