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Suppressing Plasma Induced Degradation of Gate Oxide by Using Silicon-On-Insulator Structures

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1. Introduction

One of the critical factors in the further reduction of device dimensions is the charge build-up in reactive ion etching (RIE), which causes gate breakdown in metal/oxide/silicon (MOS) devices. As far as the electrical damage due to charge build-up is concerned, discussions from the viewpoints of plasma uniformity have been reported.[1,2] From this point of view, we found that electrically negative gases such as O_2 and CF_4 tend to produce nonuniform plasma and result in pronounced charge build-up.[3]

On the other hand, from the viewpoints of the design of device structures to reduce the charge build-up, we found that the charge build-up can be drastically reduced by using silicon-on-insulator (SOI).[4] In the previous study, the charge build-up was evaluated by using metal/nitride/oxide/silicon (MNOS) capacitors fabricated on SOI.

In this study, we report that the use of SOI structures, in fact, suppresses plasma induced degradation of gate oxide. The degradation of gate oxide is evaluated by the reduction of charge-to-breakdown (ΔQ_{bd}) of the gate oxide with a constant current stress. SOI wafers prepared by the direct bonding are used. It is shown that increase in buried oxide thickness results in less degradation of gate oxide. An electrical model to explain the effect of SOI is discussed.

2. Experimental

MOS capacitors fabricated on SOI were used to evaluate degradation of gate oxide by plasma induced charge build-up. The structure of this test devices is shown in Fig. 1.

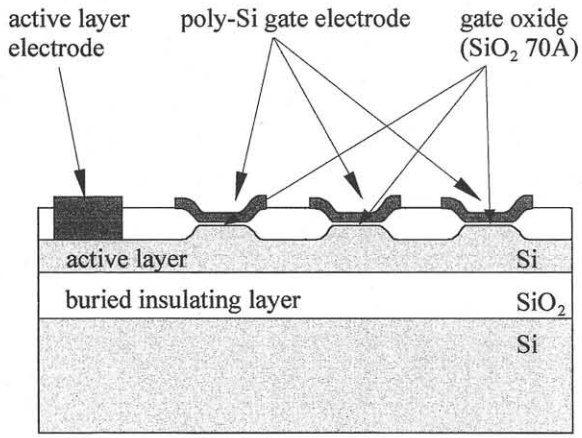

Fig. 1: Schematic cross section of MOS capacitors on SOI.

The charge-to-breakdown Q_{bd} of the MOS capacitors was measured with the constant current of 100 mA/cm^2. In order to investigate the dependence of the charge-to-breakdown Q_{bd} on the thickness of the buried oxide layer, SOI wafers having buried oxide layer ranging from 0.33 to 2.94 μm in thickness were prepared by the direct bonding. The structural parameters of this test device are listed in Table I. A parallel plate RIE system was used. The wafers were placed on the cathode with a quartz cover. Oxygen plasma was generated by applying radio frequency (13.56MHz) power. Detail of plasma treatment condition is listed in Table II. This plasma condition was used because it caused a high charge build-up.[3]

Table I. MOS capacitor specifications.

Thickness of gate oxide	70 Å
Thickness of poly-Si gate	2500 Å
Thickness of buried SiO_2	0 (bulk), 0.33, 0.94, 2.94 μm
Gate oxide area	100 μm^2
Antenna ratio	10000

Table II. Plasma treatment conditions.

Gas	O_2
Gas flow rate	50 sccm
RF power	50 W (80 mW/cm^2)
Plasma exposure time	0, 5, 10, 15 min
Pressure	10 Pa

3. Results and Discussion

Figures 2(a) and 2(b) show cumulative failure versus charge-to-breakdown Q_{bd} for bulk and SOI structure with plasma exposure time of O_2 plasma in the Weibull plots. We can see from this figure that the Q_{bd} obtained for the bulk device drastically decreases with the increase of plasma exposure time. On the other hand, it can be seen that the Q_{bd} obtained for SOI device is almost the same as that of intrinsic gate oxide. These results clearly demonstrates that plasma induced degradation of gate oxide can be drastically reduced by using the SOI structure.

Figure 3 shows variation of average Q_{bd} for bulk and SOI devices with exposure time. Results obtained from SOI wafers having various buried oxide thickness were plotted. We can see from this figure that the thicker buried oxide of the SOI devices gives the less oxide degradation. The slope of the plot

gives the reduction in charge-to-breakdown ΔQ_{bd} with exposure time. [5] In the case of bulk device, the slope is about 1 C/cm^2/min. From this value the tunneling current through gate oxide due to charge build-up during plasma exposure is estimated to be about 17 mA/cm^2. On the other hand, the tunneling current for the SOI device having 2.94 μm-thick buried SiO_2 is estimated to be only about 0.7 mA/cm^2 on the average.

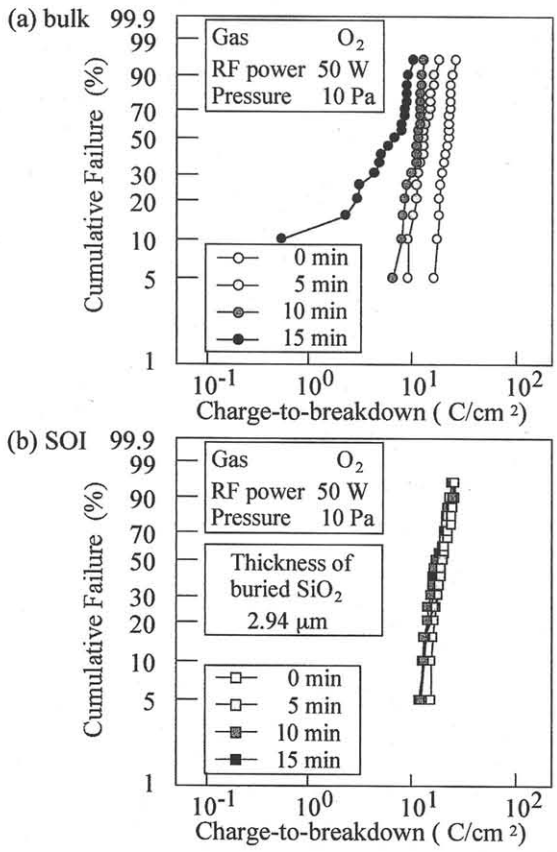

Fig. 2: Charge-to-breakdown characteristics of (a) bulk device and (b) SOI device.

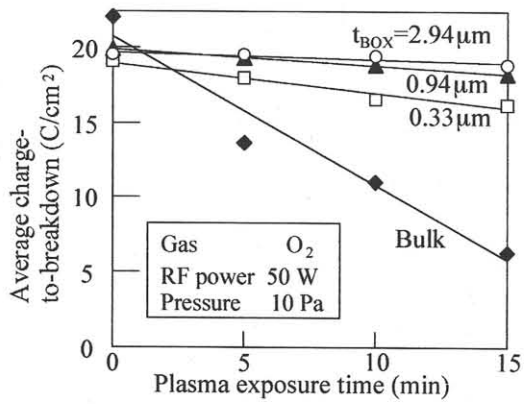

Fig. 3: Variation of average Q_{bd} for bulk and SOI device with exposure time of O_2 plasma. Results obtained for SOI devices having various buried oxide thickness are plotted.

The suppression of plasma induced degradation of gate oxide by the use of SOI can be explained by the equivalent circuit model shown in Fig. 4(a). That is, SOI provides a capacitor C_{BOX} of the buried oxide in addition to the device (MOS) capacitor. These capacitors are connected in series between the plasma and the cathode of the plasma equipment. On the surface of the wafer, the metal electrode of the MOS capacitor collects the plasma current from current source I_{PLAS}. The collected current causes the voltage of the metal electrode to increase with respect to the active layer or the substrate. The increase in voltage increases current through the gate insulator. This current would be the Fowler-Nordheim tunneling current in a conventional metal-oxide-silicon (MOS) system. Thus, we designate this current I_{FN} in Fig. 4. The current I_{FN} charges the capacitor (C_{BOX}) of buried SiO_2 and increases the potential of the active layer. As a result, the effective voltage applied to the gate capacitor is reduced. Therefore, charge build-up can be reduced by increasing the buried SiO_2 thickness, because the capacitance C_{BOX} decreases. In the case of the bulk device, on the other hand, the potential of the substrate is not increased, since I_{FN} flows out through the Si substrate to the cathode of the plasma system and then to the plasma. [6]

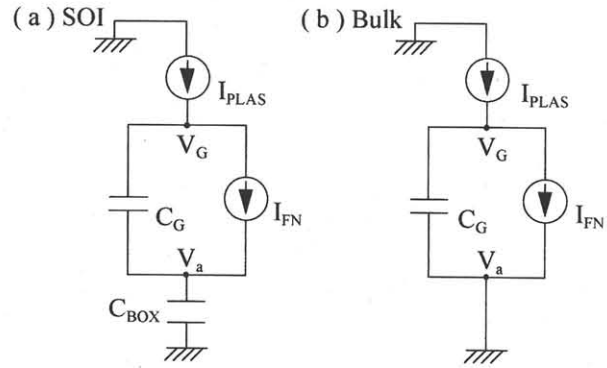

Fig. 4: An equivalent circuit model for charging in (a) SOI device and (b) bulk device.

4. Conclusion

We conclude that the use of SOI structures is very effective in suppressing plasma induced degradation of the gate oxide during plasma processing. The suppression of the degradation of the gate oxide by the use of SOI can be explained by an electrical model in which the buried oxide provides a capacitor in addition to the device capacitor and, therefore, the potential across the gate oxide is reduced by the charging. Thus, the thicker buried oxide shows more effective suppression of the gate oxide degradation. This is in fact experimentally observed. Investigation of SOI devices on SIMOX wafers is in progress.

References

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