Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 148-149

Precise Measurement of Strain in SOI Induced by Local Oxidation

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1. Introduction

Strain induced by the local oxidation of silicon (LOCOS) process has become a serious problem since LSI device dimensions are continuously shrinking [1]. In the case of thin-film SOI devices, the strain is expected to be especially great because the device region is fully isolated by surrounding SiO_2 on all sides except for the surface. This may degrade SOI device characteristics such as the gate oxide integrity and leakage current at the LOCOS edge [2,3]. Therefore, we have used X-ray diffraction to study the strain in SOI wafers that is induced by LOCOS process when used to fabricate 64M dynamic random access memories (DRAMs). With plasma assisted chemical etching (PACE) processed SOI wafers as samples, the reflection peaks of the top Si layer and base Si substrate can be measured independently since the orientation of these lattice planes differs slightly, and the strain near the surface region can be measured since the top Si layer is only a few hundred nanometers thick. We have successfully analyzed the strain in the top Si layer quantitatively and found that the strain was strongly affected by the isolation structure used.

2. Experimental Procedure

Samples were PACE-processed SOI wafers with and without LOCOS structures. Schematic figures of the samples are shown in Fig. 1. Sample A is an as-received <001>-oriented wafer with a 200-nm-thick p-type (4.5-6 Ωcm) top Si layer, a 1.5-μm-thick buried oxide (BOX) layer, and a 675-μm-thick p-type (13.5 Ωcm) base Si substrate. On samples B and C, LOCOS structures were fabricated. First, a pad oxide film (~50 nm) and a silicon nitride film (~160 nm) were grown then patterned for a 64M DRAM with a 0.4-μm-rule field mask [4]. After that, a field oxide film with a thickness of about 200 nm (sample B) or about 450 nm (sample C) was grown by wet thermal oxidation at 1000°C. Thus, sample C had an isolated structure, consisting of Si islands surrounded by SiO_2 on all sides except the surface. The samples B and C were confirmed to have the expected LOCOS structures by scanning electron microscopy and transmission electron microscopy.

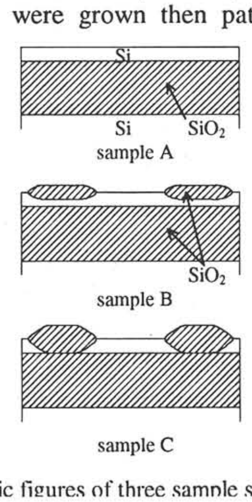

Fig. 1. Schematic figures of three sample structures.

We performed X-ray diffraction measurements using a high-resolution X-ray diffractometer (Rigaku SLX-2000) with two channel cut Ge monochrometors [5,6] of 220 symmetric reflections in the (− + + −) arrangement. Rocking curves of the samples were taken for a 004 symmetric reflection with an ω-scan using a 0.0002° step size and Cu$K\alpha_1$ radiation from a rotating anode X-ray generator operating at 50 kV and 300 mA. Two rocking curves were taken for each sample by rotating the sample around the normal to the sample surface (the ϕ axis). Two sample orientations ϕ_- and ϕ_+, were found so that the angular difference between the top Si layer and the substrate peak positions in the rocking curve indicates a maximum. When the top Si peak appeared on the lower angle side of the substrate peak, the sample orientation was defined as ϕ_-, and the opposite case was defined as ϕ_+, where $|\phi_+ - \phi_-| = 180°$. For each sample, the difference between the (004) plane spacing of the top Si layer and that of the substrate, where the plane spacing of the substrate is the same before and after the LOCOS process, is determined as [7]

$$\frac{\Delta d}{d} = -\frac{\Delta\omega_- + \Delta\omega_+}{2}\cot\theta_B , \qquad (1)$$

where $\Delta\omega_-$ and $\Delta\omega_+$ are the angular differences (in units of radians) between the top Si layer and the substrate peak positions measured at the sample orientations ϕ_- and ϕ_+, respectively, and θ_B is the Bragg angle.

3. Results and Discussion

Figures 2(a)-2(c) show the experimental rocking curves of samples A , B and C, respectively, where Δω represents the angular deviation from the substrate peak position, and the upper and lower rocking curves were taken at the sample orientations ϕ_- and ϕ_+, respectively. In Fig. 2(a), both peaks of the substrate and the top Si layer are clearly observed. The peak of the top Si layer shows clear oscillations (finite thickness fringes), indicating that both the crystalline quality and thickness uniformity of the top Si layer is high. Furthermore, $\Delta d/d$ calculated using eq. (1) is almost zero (Table I). These results show that as-received PACE-processed SOI wafers have strain-free top Si layers.

In the case of sample B [Fig. 2(b)], although the rocking curves show two peaks, the peak of the top Si layer is broader than that in Fig. 2(a) and it shows no clear oscillations. This is due to non-uniform strain and thickness in the top Si layer due to the LOCOS fabrication. We calculated the average $\Delta d/d$ to be $+1.7 \times 10^{-4}$ (Table I), which indicates that strain induced by the LOCOS process expanded the top Si layer perpendicular to the surface by about 0.017%. This caused the areas surrounded by SiO_2 films in the top Si layer to be compressed parallel to the surface due to the volume increase caused by local oxidation. Since

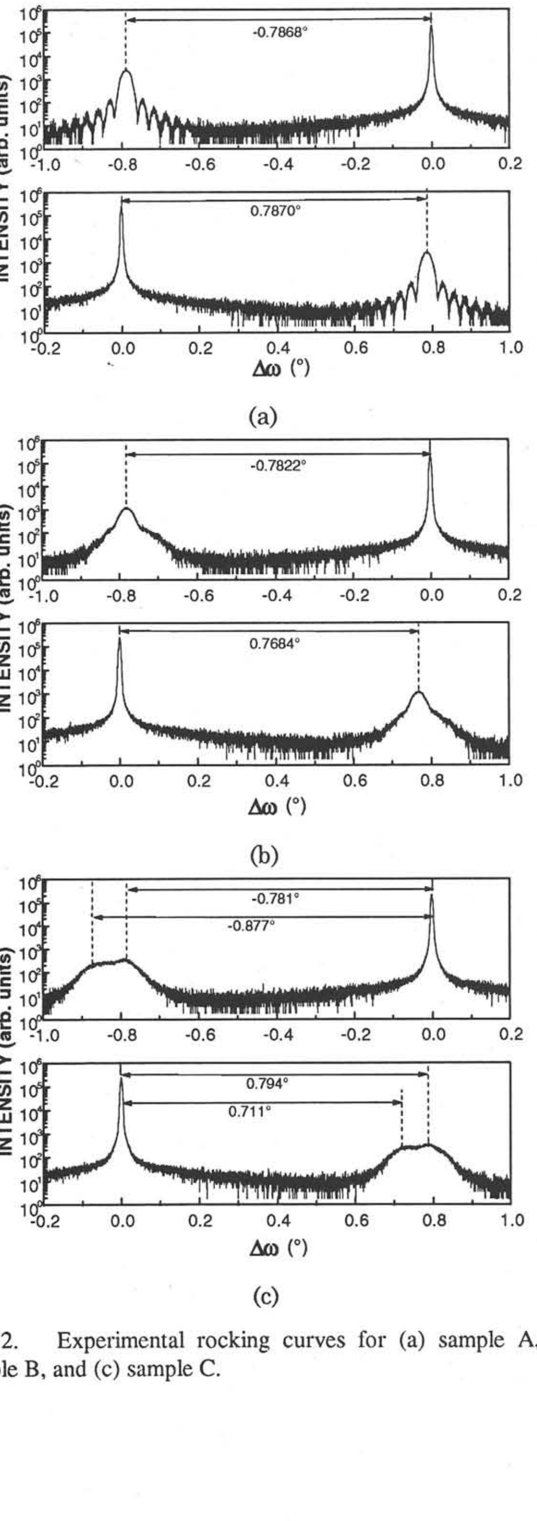

Fig. 2. Experimental rocking curves for (a) sample A, (b) sample B, and (c) sample C.

Table I $\Delta d/d$ of the samples

Sample	$[(\Delta\omega_- + \Delta\omega_+)/2]$ (°)	$(\Delta d/d) \times 10^{-3}$
A	$+0.0001 \pm 0.0002$	-0.003 ± 0.005
B	-0.0069 ± 0.0004	$+0.17 \pm 0.01$
C (peak 1)	-0.083 ± 0.001	$+2.10 \pm 0.03$
C (peak 2)	$+0.007 \pm 0.001$	-0.18 ± 0.03

the LOCOS structure of this sample is not unique to SOI wafers, we expect a similar strain to be induced in bulk wafers by the LOCOS process.

In the case of sample C [Fig. 2(c)], the substrate peak is almost the same as that in Fig. 2(b), but the peak of the top Si layer is much broader than that in Fig. 2(b) and splits. This indicates that the LOCOS structure of sample C, which is an isolation structure unique to SOI wafers, causes different types of strain in the top Si layer. The calculated $\Delta d/d$ for the lower angle side peak (hereafter referred to as peak 1) and the higher angle side peak (peak 2) is $+2.1 \times 10^{-3}$ and -1.8×10^{-4}, respectively (Table I). This result shows that two regions, one that expanded by about 0.21% and one that shrank by about 0.018%, co-exist in the top Si layer of sample C. Peak 2 might be reflected from the regions under the bird's beak, since the top and bottom surfaces of these regions were sandwiched and compressed perpendicularly to the surface by silicon dioxide. On the other hand, peak 1 might be reflected from the free top surface regions, since these regions were strongly compressed parallel to the surface by the LOCOS regions. The expansion of the regions was more than ten times greater than that of the top Si layer of sample B. This indicates that the strain induced by the LOCOS process is a much more serious problem for thin-film SOI devices.

4. Summary

We quantitatively measured the strain induced by the LOCOS process in the top Si layers of PACE-processed SOI wafers by X-ray diffraction. We found that the strain in SOI wafers is more than one order of magnitude larger than that in bulk wafers when the device region is fully isolated by surrounding SiO_2 on all sides except the surface.

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