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Sub-0.25 μm Devices and 16K SRAM with Selective-Epi Source/Drain on Ultra-Thin SOI

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1. Introduction

To insure completely (not "nearly") fully depleted behavior (1) and also prevent transient floating body effects, the silicon thickness of fully-depleted sub-0.25μm SOI devices must be less than 500Å. This leads to increased series resistances which, on such thin layers, cannot be corrected by the widely used self-aligned silicidation process. To overcome this problem, we used selective epitaxial source / drain (2) to fabricate sub-0.25μm devices and for the first time a 16K SRAM on ultra-thin (≈ 350Å) SOI.

2. Process description

Different SIMOX wafers were used having low, medium and standard implant dose (800Å, 1500Å and 3800Å of buried oxide, respectively) with differing initial silicon thicknesses. After silicon thinning and LOCOS isolation, a single N+ gate process was used to obtain enhancement-mode (EM) NMOS and accumulation-mode (AM) PMOS devices with 45Å gate oxide. The gate level was patterned with mixed E-Beam and DUV lithography. The poly-Si gate etching was followed by the formation of a 0.1μm TEOS spacer. Then, silicon was selectively deposited at 850°C, after a hydrogen prebake at the same temperature. Owing to a spacer shrink at the top of the gate during the process, silicon grew laterally into a "mushroom" shape (Fig. 1). This could be avoided by optimizing the gate stack or the spacer processes.

3. Experimental results

Source / drain sheet resistance varies with silicon thickness, as shown in Fig. 2 for NMOS. It is about two times higher for PMOS. A similar result was obtained with a recessed channel (RC) process (3). Unlike RC, selective epitaxy (SE) is self aligned between the gate and the source/drain. Asymmetry can be compared by measuring the difference between saturation currents when source and drain are inverted. Since the linear current strongly depends on series resistances (4), it can be drastically reduced where poor overlay results in a wide ultra-thin region between the gate and the adjacent thick silicon area. The large current range in the SE case (Fig. 3) is not due to asymmetry; it is caused by different source/drain extension implant doses. Whereas asymmetry is less than 10% in the SE case, it can be higher than 50% in the RC case. In the present case, the high RC asymmetry can be explained by a die-to-die shift in E-Beam offset for the gate level. This could be improved but it emphasizes that the RC structure (Fig. 4) requires stringent overlay specifications (mean +/- 3 sigma ≈ 0.12μm). Typical Id(Vd) curves obtained with SE structure are shown in Fig. 5. The measured source and drain sheet resistances per square are 200 Ω and 450 Ω for N+ and P+ regions respectively. This could be reduced by increasing epi-thickness as shown in Figure 2. The PMOS drive current could be enhanced by decreasing the threshold voltage Vt (Fig. 6). In the case of NMOS a leakage current was observed because the isolation process had not been optimized. Short channel effects (SCE) for NMOS (Fig. 7) depend on the substrate. These results are due to differing silicon thicknesses under the gate at the end of the process. The medium dose substrate, having the thickest channel, exhibits higher roll-off whereas the low-dose substrate has the thinnest channel and consequently the best SCE behavior. It is interesting to note that Vt is independent of thickness for 0.2μm gate length because of a balance between Vt increasing for a long channel device and worse SCE when silicon is thicker. It means that EM fully-depleted devices with ultra-thin films are therefore not too much sensitive to thickness non uniformity. Nevertheless, in the AM case, no balance is available: Vt decreases with a thicker film but SCE is worse too. This suggests that dual gates would be a better choice for the spread issue. Dynamic performance was measured on ring oscillators with 0.8μm design rules (Fig. 8). The gate delay results (tp = 75ps @ 2V for 0.25μm gate length) are quite similar to those obtained with same design and RC structure (3). To further demonstrate the advantages of SE, a 16K SRAM with 0.5μm gate length was fabricated with the same process, and performed to specifications. Fig. 9 shows the access time TAA as a function of supply voltage (TAA = 14ns @ 1.8V). These results demonstrate for the first time the low voltage operation of SOI/CMOS SRAM circuits with a selective-epi elevated source/drain structure.

4. Conclusion

Although dynamic performances could be further optimized, with lower Vt, thicker epi-film and real 0.25μm design rules, we have demonstrated that selective epi-source/drain is a viable way to obtain complete fully-depleted devices. Dynamic results on ring oscillators and 16K SRAM are available for the first time on ultra-thin film SOI substrate with selective-epi source/drain structure.

References

(1) L. Su et al, IEEE SOI Conference Proceedings, p 112, 1993
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(3) C. Raynaud et al, IEEE SOI Conference Proc., p 80, 1996
(4) O. Faynot et al, IEEE Electron Device Letters, p174, 1994

Acknowledgments

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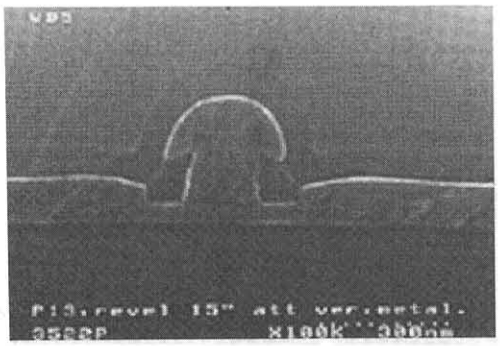

Figure 1 : Selective-epi source / drain structure

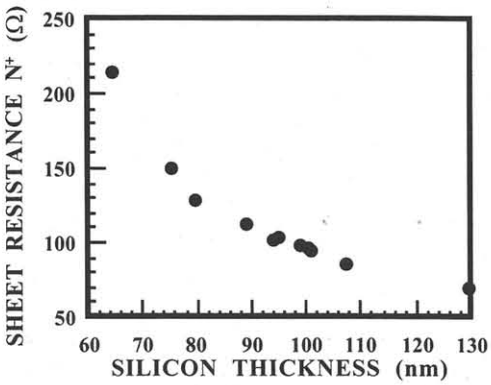

Figure 2 : Sheet resistance versus silicon thickness

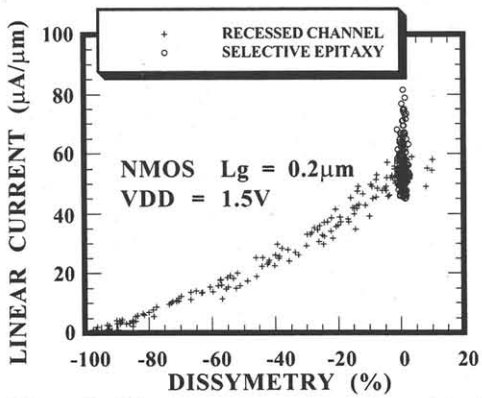

Figure 3 : Linear current versus source / drain dissymetry

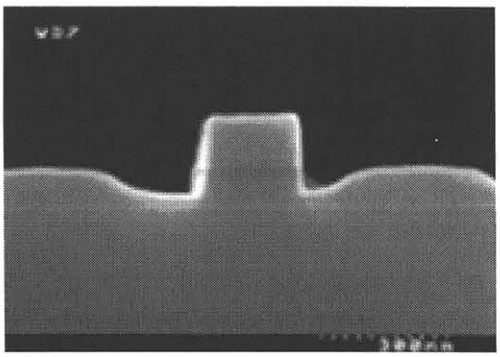

Figure 4 : Recessed-channel structure

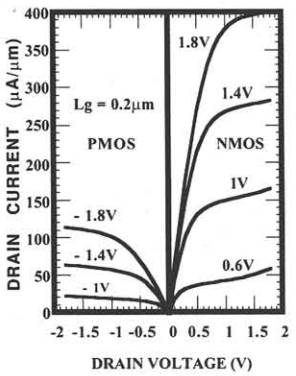

Figure 5 : Id(Vd) curves

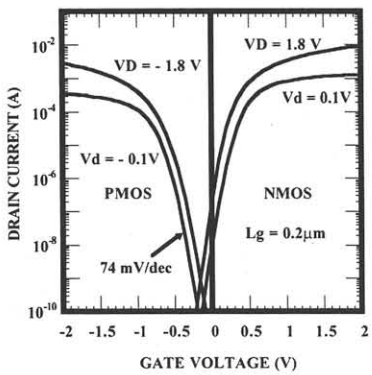

Figure 6 : Id(Vg) curves

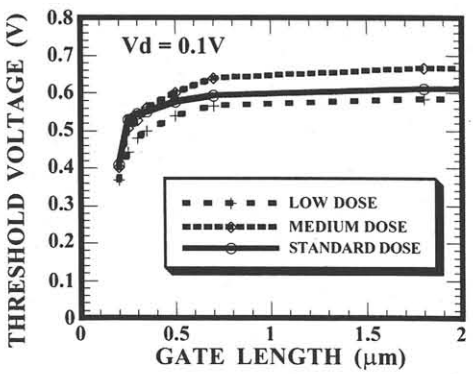

Figure 7 : SCE for different substrates

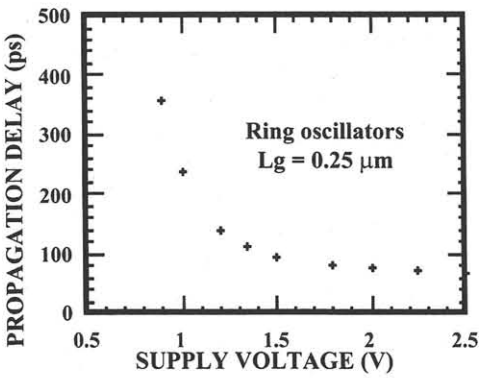

Figure 8 : Ring oscillators propagation delay versus supply voltage (0.8µm design rules)

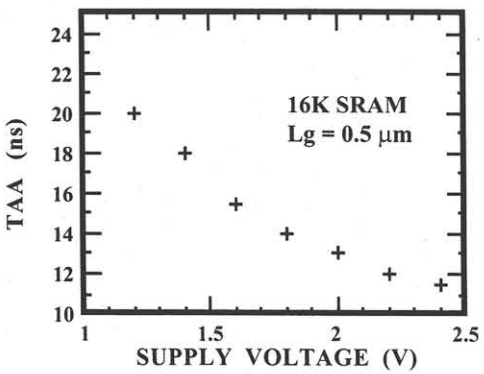

Figure 9 : 0.5µm 16K SRAM access time TAA as a function of supply voltage