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Non-Stationary Electron/Hole Transport in Sub-0.1 μm MOS Devices -Degradation Mechanism and Low-Power Applications-

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I. INTRODUCTION

In previous works [1,2], we experimentally verified that electron velocity overshoot is achieved in sub-0.1 μm SOI-MOSFETs when gate drive is low, and high performance operation can be realized by using the velocity overshoot effect at a low supply voltage.

In this study, we have experimentally compared hole and electron velocities in the sub-0.1 μm region using SOI and bulk MOSFETs. We clarify the physical mechanism for the carrier velocity degradation of both electrons and holes. In addition, we discuss design for low-voltage operation using the velocity overshoot in sub-0.1 μm CMOS devices.

II. EXPERIMENTAL

0.08 μm fully depleted SOI CMOS devices were fabricated on a SIMOX wafer. The gate oxide, the SOI layer, and the buried oxide thicknesses were 4.4 nm, 40 nm, and 100 nm, respectively. The Ni salicide structure was adopted to reduce the source/drain parasitic resistance. Bulk CMOS devices were also fabricated by the 0.1 μm CMOS process [3]. The effective vertical field dependence of the low-field mobility μ was found to be almost the same as that of the universal curve [4].

III. RESULTS AND DISCUSSION

In this work, we experimentally obtain the carrier velocity v near the source using $v(V_{GT}) = I_D(V_{GT})/(\int^{V_{GT}} C_{gs}(V'_{GT})\mathrm{d}V'_{GT})$, where C_{gs} is the gate-to-source capacitance [1,2,5] and V_{GT} is the gate drive. Figure 1 shows the relationship between v and the gate drive in CMOS SOI devices. In $L_{eff} = 0.08$ μm, the maximum values of the electron velocity v_e and the hole velocity v_h are 1.3×10^7 cm/s and 7.0×10^6 cm/s, respectively. It is found that both v_e and v_h degrade with increasing gate drive in $L_{eff} \leq 0.2$ μm. Moreover, the L_{eff} dependence of v_e and v_h for the SOI and bulk MOSFETs is shown in Fig. 2. We find that the power of the L_{eff} dependence in holes is larger than that in electrons. In a smaller gate drive, the power of the L_{eff} dependence of v is found to be larger. It is considered that v_h will be higher than 1×10^7 cm/s at $L_{eff} = 0.05$ μm.

In order to analyze the physical mechanism for v degradation, we studied the intrinsic v_e and v_h as a function of μ, where the intrinsic velocity is obtained by considering the self-heating and the parasitic resistance. Figure 3 shows the μ dependence of v translated from the V_G and V_{SUB} dependence of v. For $L_{eff} \leq 0.18$ μm, the μ dependence of v obtained from the V_G dependence is almost the same as that obtained from the V_{SUB} dependence, which indicates the carrier velocity is independent of the carrier density [5]. It is to be noted that, at the same L_{eff}, both v_e and v_h have the universal μ dependence, that is , $v \propto \mu^{\alpha}$. This means that both low v_h and v degradation in high gate drive are due to μ degradation. The power of the μ dependence at 0.08 μm is larger than that at 0.13 μm, which is due to non-stationary effects.

Figure 4 shows the relationship between $1/v$ and L_{eff}, as a parameter of μ. We obtain the L_{eff} dependence of v based on linear fitting of the $1/v - L_{eff}$ relation. The contour map of v in the relationship between μ and L_{eff} is shown in Fig. 5. It is found that the μ dependence of v is more marked for shorter L_{eff}. We also find that, for shorter L_{eff}, the critical mobility for velocity overshoot exceeding $v_{sat} = 1 \times 10^7$ cm/s becomes lower. Indeed, the critical μ is given by $\mu = 22.1$ [cm^2/Vs] $\times \exp(30.6$ [μm^{-1}] $\times L_{eff})$. Since $\mu \sim 100$ cm^2/Vs in pMOSFETs, L_{eff} must be less than 0.05 μm to attain velocity overshoot.

Next, we discuss design for low-power operation. The power supply voltage V_{dd} conditions to achieve the velocity overshoot are shown in Fig. 6. Figure 6(a) shows that, in the case of electrons, $V_{dd} = 0.5$ V is the most suitable for high-speed operation using the velocity overshoot. In the higher V_{dd} region, v_e decreases according to the mobility reduction as shown in Fig. 3. Hence, the electron velocity overshoot is suitable for low-power applications, such as less than 1 V. However, in Fig. 6(b), we note that 1.25 V supply voltage is the most effective for high-speed operation in pMOSFETs, because higher drain bias must be applied to get a higher hole velocity. This means that, in CMOS operation, the most suitable V_{dd} is about halfway between 0.5 V and 1.25 V, that is, $V_{dd} \sim 0.9$ V.

IV. CONCLUSION

We studied the high-field carrier velocity of both electrons and holes in the sub-0.1 μm region. We demonstrated that both v_e and v_h have universal μ dependence at the same L_{eff}. We experimentally obtained the critical mobility to achieve velocity overshoot, that

is, $\mu = 22.1$ [cm^2/Vs] $\times$ exp(30.6 [μm^{-1}] $\times$ L_{eff}). Moreover, we introduce the design for low-voltage operation using the velocity overshoot. The most suitable supply voltages are 0.5 V and 1.25 V for electrons and holes, respectively, and in CMOS, 0.9 V is the most suitable.

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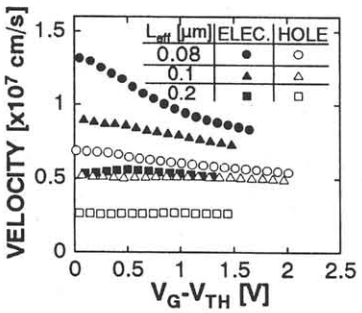

Fig.1 Carrier velocity v *vs.* gate drive for SOI CMOS devices with L_{eff} = 0.08, 0.1, and 0.2 μm, where $|V_D| = 1$ V and $|V_{SUB}| = 8.5$ V. v degrades with increasing gate drive.

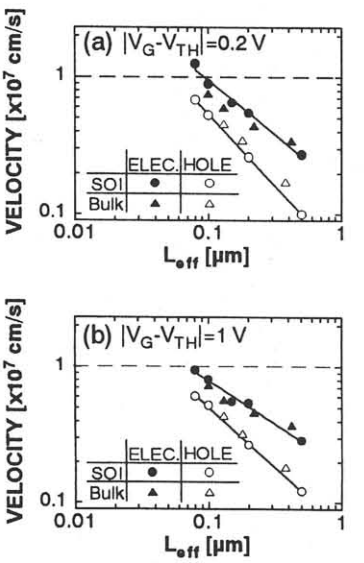

Fig.2 L_{eff} dependence of the carrier velocity v at (a) $|V_G - V_{TH}| = 0.2$ V and (b) $|V_G - V_{TH}| = 1$ V in SOI and bulk CMOS devices, where $|V_D| = 1$ V, and $|V_{SUB}| = 8.5$ V and 0 V in SOI and bulk, respectively.

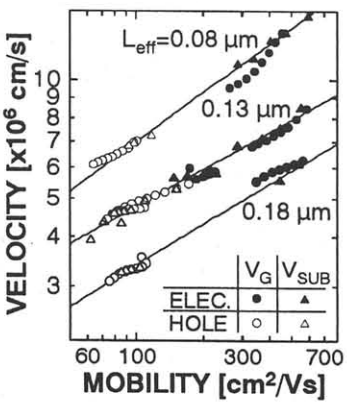

Fig.3 Carrier velocity v *vs.* low field mobility μ for 0.08, 0.13, and 0.18 μm CMOS devices with SOI and bulk structures, where $|V_D| = 1$ V. The μ dependence of v was independent of the MOS structure. The $v - \mu$ relations obtained from V_G and V_{SUB} dependence are indicated by circles and triangles, respectively. Both of the v degradation and low v_h are due to the mobility reduction.

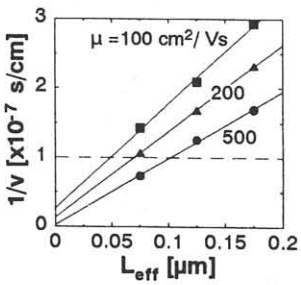

Fig.4 L_{eff} dependence of $1/v$ as a parameter of μ, where $|V_D| = 1$ V. We obtain the L_{eff} dependence of v based on the linear fitting.

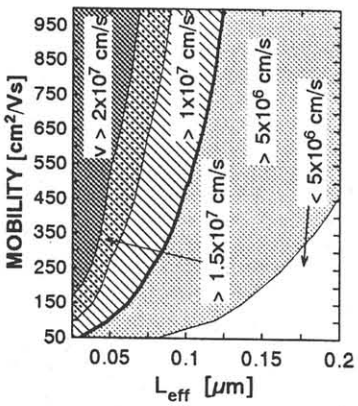

Fig.5 Contour map of v in the relationship between L_{eff} and μ, where $|V_D| = 1$ V. The critical μ to achieve 1×10^7 cm/s is lower in shorter L_{eff}, and given by μ = 22.1 [cm^2/Vs] $\times$ exp(30.6 [μm^{-1}] $\times$ L_{eff}).

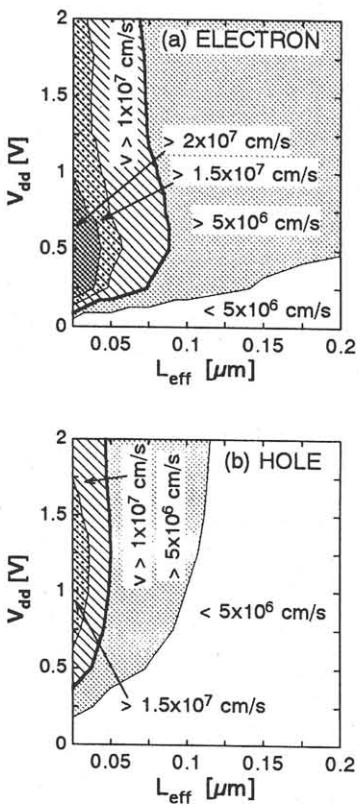

Fig.6 L_{eff} dependence of design for supply voltage V_{dd} in (a) electrons and (b) holes, where $V_{dd} = V_D = V_G - V_{TH}$. 0.5 V and 1.25 V supply voltages are the most suitable in electrons and holes, respectively. In CMOS devices, 0.9 V operation is the most suitable.