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A Hybrid Lateral SOI BMFET with High Current Gain

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1. Introduction

The Bipolar-Mode Field-Effect Transistor (BMFET) attracts a considerable interest because of its high current density, extremely low on-resistance and fast switching speed[1]. It has reported that the lateral SOI BMFET may be a promising power switching devices for power IC applications[2]. However, conventional SOI LBMFET suffers from the low current gain, so the operation is limited to the low current area.

The purpose of our work is to propose a novel hybrid-mode Lateral SOI BMFET with high current gain by employing a lateral bipolar transistor and a DMOS structure. The operations of the proposed BMFET are verified by device simulation by using MEDICI.

2. Device Structure and Operation

The cross-sectional view of the conventional SOI LBMFET and the proposed device are shown in Fig. 1. The lateral SOI BMFET's are basically lateral JFET structures with the channel formed between buried oxide and deep p^+ gate junction.

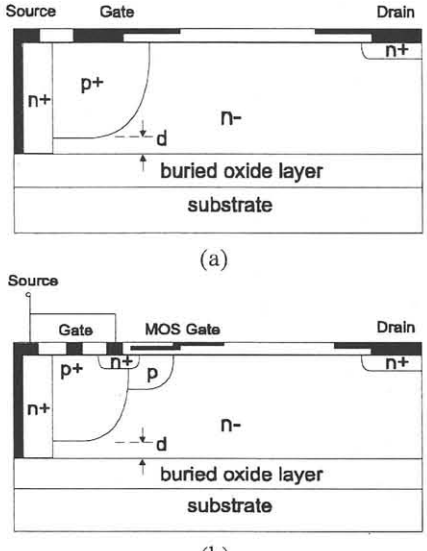

Fig. 1.Cross-sectional view of (a) the conventional BMFET and (b) the proposed BMFET with a DMOS structure

The proposed device can be operated in three modes. The hybrid mode is implemented by connecting p^+ gate and MOS gate together[3]. The hybrid mode effect is due to gate-induced lowering of effective base charge, resulting in a reduction of emitter-base junction barrier and high current gain. BMFET mode and DMOS mode are implemented by connecting MOS gate and p^+ gate to source, respectively.

The 4 μm thick, 5×10^{13} cm^{-3} n-type silicon layer on the 2 μm buried oxide and 5×10^{13} cm^{-3} p-type substrate is employed in the 2-dimensional device simulation. The doping profile is assumed to be gaussian and the normally-off behavior obtain by 1 μm channel depth. The device parameters employed in the device simulation is listed in Table I.

Table I. Device parameters used in the simulation

parameters		value
surface doping	n^+ source	1×10^{20} cm^{-3}
	p^+ gate	1×10^{19} cm^{-3}
	p-body	5×10^{16} cm^{-3}
n^- drift region doping		5×10^{13} cm^{-3}
thickness	SOI layer	4 μm
	buried oxide	2 μm
	gate oxide	500 Å
p-body junction depth		2 μm
n^+ source junction depth		0.5 μm
drift region length		20 μm
channel depth (d)		1 μm
SRH lifetime coefficients	τ_{no}	1×10^{-7} sec
	τ_{po}	1×10^{-7} sec
	N_{SRHn}	4×10^{16} cm^{-3}
	N_{SRHp}	1×10^{16} cm^{-3}

3. Simulation Results and Discussion

The simulated transfer curves for various modes are shown in Fig. 3. Our simulation result shows that the current gain of hybrid mode operation is at least 10 times larger than that of BMFET mode. The threshold voltage of DMOS structure is about 0.6 V and the subthreshold swing is 115 mV/dec.

Fig. 4 illustrates the simulated band diagram perpendicular to the p-body/gate-oxide interface for hybrid and BMFET mode when V_{ds} = 5 V and V_{gs} = 0.5 V. The emission barrier is lowered when the device is operated in

the hybrid mode. The corresponding (b). The depletion region extends to about 1000 Å into p-body from the gate oxide interface and reduction of the emission barrier occurs in this region.

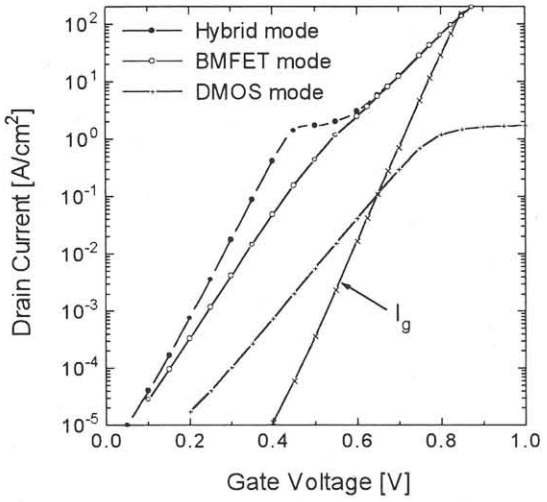

Fig. 3. Simulated transfer curves of the proposed device

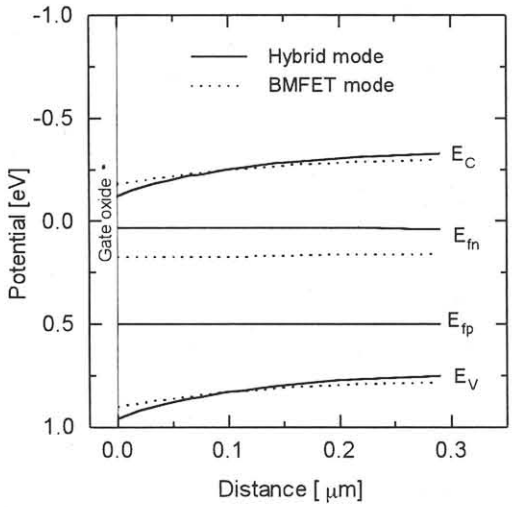

Fig. 4. Simulated band diagram through the p-body perpendicular to the p-body/gate-oxide interface at V_{ds} = 5 V.

The current gain of the proposed device is compared with the previously reported SOI LBMFET in Fig. 5. The current gains of over 30000 can be achieved in hybrid mode operation. It can be seen that the current gain peak of proposed device in hybrid mode is 30 times larger than that of previously reported lateral SOI BMFET.

The forward voltage drop of hybrid LBMFET is 0.1 V at the current density of 20 A/cm^2, while those of LIGBT and LDMOS on the same SOI substrate are 0.9 V and more than 5 V, respectively as shown in Fig. 6. The forced gate turn-off simulation is implemented in condition that the anode voltage is 100V and the resistive load is employed. From these results, LIGBT shows the longer turn-off time even at the condition of smaller lifetime. However, the simulated turn-off time of proposed device is 0.2 μsec without the long tail current, which is comparable to LDMOS.

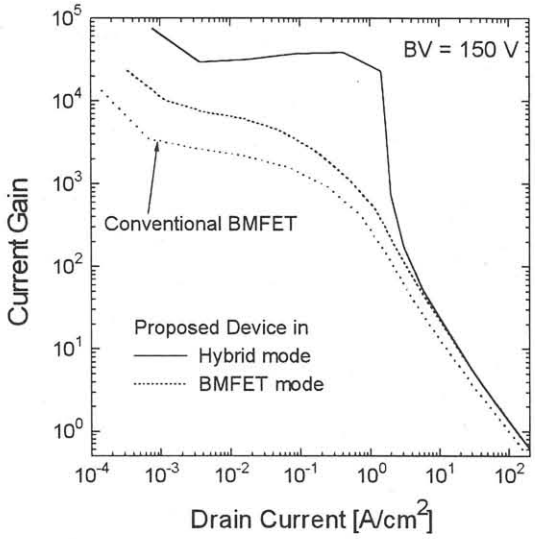

Fig. 5. Comparison of Current gain for different device structures at V_{ds}= 5V.

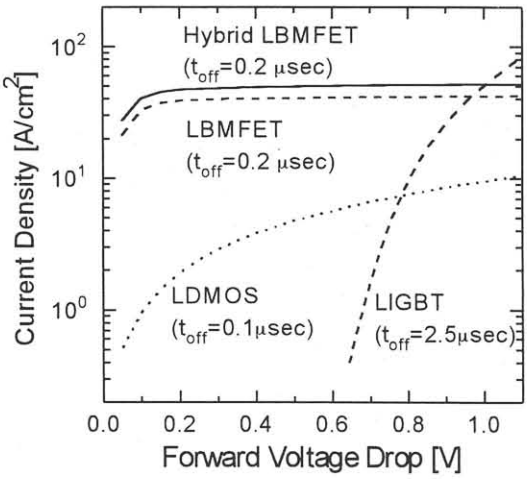

Fig. 6. Comparison of forward voltage drop, current density and turn-off time among the various lateral devices.

4. Conclusion

The high current gain hybrid BMFET with DMOS structure is proposed and verified by device simulation. The simulation results show that the proposed BMFET improves current gain significantly by hybrid mode operation, compared with the conventional device. The proposed device shows current gains over 30000, which is 30 times larger than the conventional LBMFET.

References

1) A. Caruso, et. al. : IEEE Trans. on Power Electronics, vol. 3 (1988) p 157.
2) S. D. Kim et al. : Proc. of ISPSD'95 (1995) p 288.
3) J. Olsson et. al. : IEEE Trans. Electron Devices, vol. 42 (1995) p 1628.