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Long-Term Reliability of the Blocking Capability and Failure Voltage of Electrostatic Discharge(ESD) of SOI High-Voltage Device and IC

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1. Introduction

Dielectric isolation using a silicon-on-insulator(SOI) wafer is a promising technology for high-voltage power ICs. Owing to strenuous efforts to develop device and process technologies[1,2] SOI high-voltage power ICs(SOI-ICs) have become commercially available.

For practical use of the SOI-IC, its reliability must be ensured. Especially, it is necessary for high-voltage power ICs to accomplish the long-term reliability of the blocking capability of output devices. And the voltage required to induce electrostatic discharge(ESD) damage, that is the failure voltage of ESD, is an important factor for reliability of the IC.

This presentation reports experimental results of the reliability testing of the SOI high-voltage device(SOI-device) and SOI-IC. We have estimated the long-term reliability of the blocking capability of the SOI-device through two accelerated tests, and have measured the failure voltage of ESD of the SOI-IC.

2. Reliability Testing

Table I shows stress conditions and the number of measured chips of the reliability testing. The high-temperature reverse-bias(HTRB) and temperature cycling tests assess the long-term reliability of the blocking capability of the device. Above tests are carried out as follows: 1)HTRB test; the high voltage of 250V or 200V, whose voltages are selected in view of application to a 200V-class power IC, is continuously applied to the device during 1000 hours at 150℃. The variation of the breakdown voltage is observed. 2)temperature cycling test; the device temperature is raised from -50℃ to 150℃ and then is lowered from 150℃ to -50℃ during one hour. After this cycle repeats one hundred times, the breakdown voltage of the device is measured.

The ESD test is done according to the "machine model" (EIAJ standard). Both the positive and negative polarity discharge are applied to the output pin at the output stage in the IC against ground. Same discharge is added three consecutive times.

3. Measured Devices and ICs

A conventional lateral power insulated gate bipolar transistor(IGBT) and p-channel MOSFET(PMOS) for the accelerated tests, and a 200V-class power IC for ESD were fabricated on a 10μm-thick SOI film with a 2μm-thick buried oxide film. The SOI film was the n-type silicon and its resistivity was 5 Ω•cm.

Table I Stress condition and the number of measured chips of the reliability testing

Test	Stress condition	Chips
HTRB	250V(200V), 150℃, 1000hours	20
Temperature cycling	-50℃ ⇔ 150℃/1hour, 100cycles	20
ESD	C=200pF, R=0 Ω, 3 times	5

Two cell patterns were used for the PMOS structure; the A-PMOS has the cell pattern with the drain region surrounded by the source-gate region and the B-PMOS has the reverse pattern of the A-PMOS.

An initial breakdown voltage of the IGBT is 330V. The breakdown voltage of the PMOS is controlled between 240V and 280V by the implantation dose of a p-offset layer, which is formed near the surface region of the device.

Note that the breakdown voltage of the PMOS was measured at the condition that the substrate of a SOI wafer is electrically connected to the drain terminal of the device in view of practical use[2]. The positive voltage is applied to the source terminal of the device.

Fabricated IC includes the high-voltage push-pull circuit, which consists of above IGBT and B-PMOS, at its output stage.

The failure voltage of ESD is compared with that of the IC on a junction isolated wafer (JI-IC). A measured JI-IC has the same spec as the SOI-IC. But the chip size of the JI-IC is about 1.6 times larger than that of the SOI-IC, because the high-voltage push-pull circuit at the output stage in the JI-IC consists of the n-channel MOSFET instead of the IGBT.

4. Results and Discussion

HTRB Test

Figure 1 shows the results of the HTRB test. The IGBT maintains its initial breakdown voltage after 1000 hours. The results of the PMOS depend on the cell pattern. The A-PMOS withstands the stress during 1000 hours, while the breakdown voltage of the B-PMOS deteriorates after 24 hours. The test to the B-PMOS was stopped at this time.

The tests with the applied voltage of 200V have been applied to the PMOS. The results are shown in Fig. 2. The B-PMOS with the initial breakdown voltage of 280V maintains its initial value, but the breakdown voltage of the B-PMOS with the initial breakdown voltage of 240V deteriorates. The A-PMOS with the initial breakdown voltage of 240V keeps its initial value.

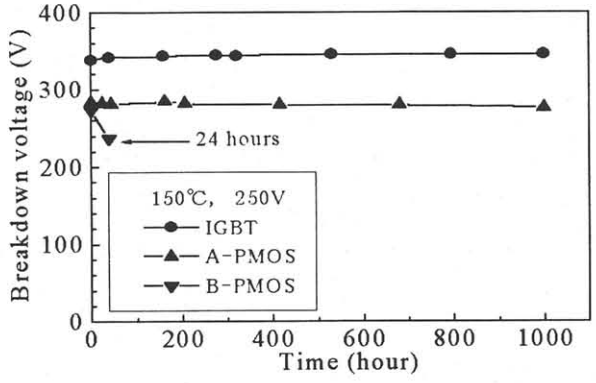

Fig. 1 Results of the HTRB test

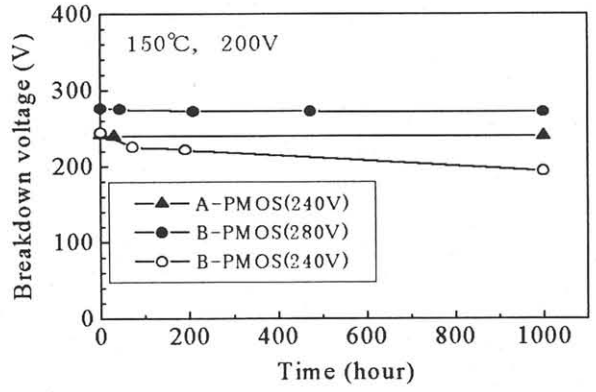

Fig. 2 Results of the HTRB test with applying the voltage of 200V to the PMOS

The results of the PMOS depend strongly on the cell pattern. The cause of this dependence is guessed as follows: avalanche breakdown in the PMOS occurs at the surface region in the p-offset layer[2], so that the long-term reliability of the blocking capability is subject to the surface structure effect of the device. When the B-PMOS pattern is adopted, a large margin to ensure the long-term reliability of the blocking capability should be necessary.

Temperature Cycling Test

The results of the temperature cycling test are shown in Table Ⅱ. In this test the breakdown voltage of the dielectric isolation, whose performance is specified by a 1μm-thick surrounding oxide film, was also measured. As shown in Table Ⅱ, all devices maintain their initial characteristics. The results of the PMOS do not depend on its cell pattern.

Table Ⅱ Results of the temperature cycling test

Device	Initial	After applying the stress
IGBT	330V	334V
PMOS	280V	285V
Isolation	740V	750V

Failure Voltage of ESD

Figure 3 shows the results of ESD. This figure indicates the ratio of the value of the SOI-IC to that of the JI-IC. The failure voltage of the SOI-IC is lower than that of the JI-IC, especially the positive polarity discharge. This may be due to the smaller chip size than the JI-IC. In general, the ESD failure depends on the junction area. Therefore high-packing density, which is one of the biggest merits of the SOI-IC, can also be a disadvantage with respect to the protection of ESD energy. However the failure voltage of the SOI-IC is over ±500V, then there is no harm in practical use.

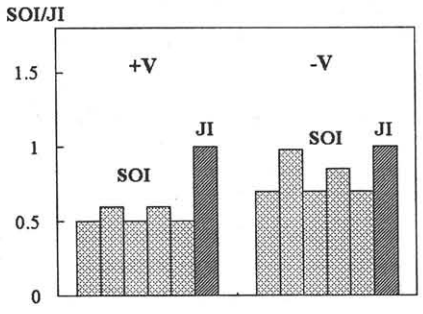

Fig. 3 Results of ESD

5. Conclusion

We have confirmed reliability of the SOI high-voltage device and IC experimentally. Two accelerated tests for the long-term reliability of the blocking capability and ESD were carried out. The SOI devices can pass two accelerated tests, but the results of the PMOS depend on its cell pattern. The failure voltage of ESD for the SOI-IC is lower than that of the JI-IC, but there is no harm in practical use.

References

1) A.Nakagawa, N. Yasuhara and Y.Baba: IEEE Trans. Electron Devices, **38**(1991)1650.

2) H. Sumida and A. Hirabayashi: Technical Report of IEICE, **SDM96-231**(1997)21