

Invited**Toward Next Generation Electronics Based on Single Electron Devices**

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1. Introduction

Tremendous progress of the LSI technology in the latter half of this century has been mainly due to progress of the fabrication technology which allowed systematic scale-down of device feature sizes and exponential growth of the integration level. This fabrication technology seems to allow production-level realization of the feature sizes of about 100 nanometer or below around the turn of the century, making device dimensions comparable with the de Broglie wavelength of electrons in semiconductors. Thus, shortly, all the devices will inevitably enter into the quantum regime. This seems to raise a fundamental question of how well the scaled-down versions of the existing devices based on semi-classical operation principle, perform in such "quantum mechanical" environments.

On the other hand, advance of such nanofabrication technology opens up an exciting possibility of constructing a novel electronics directly based on quantum mechanics in which quantum mechanical wave-particle motions of individual electrons are controlled in precisely designed artificial quantum structures such as quantum wells, wires, and dots. Since each electron manifests either wave-nature or particle-nature predominantly depending on its environment, one can conceptually envisage two kinds of electronics in the quantum regime, i.e., "quantum wave electronics" and "single electronics"[1]. In the former, electrons are put into various phase-coherent structures and their wave properties are utilized to realize various new functions. In the single electronics, on the other hand, electrons are put into "dot" structures and their particle-nature is emphasized.

The purpose of the present paper is to discuss the feasibility and the critical issues of the single electronics as a candidate for the next generation electronics. A particular emphasis is placed on the objective and current status of the Scientific Research Project on Priority Area of "Single Electron Devices and Their High Density Integration" started in Japan from April 1996 for a period of four years under the support of the Ministry of Education, Science, Sports and Culture, Japan. In this project, intensive collaborative efforts are being sought among researchers in the material/device related fields such as basic physics, electron device physics, material science, processing engineering, etc., and those in the system related fields such as circuit and system engineering, computer science, neural networks, etc., in order to find ways to future in the vast open fields of "quantum regime" where no well established "Roadmap" such as the famous one for the Si technology by Semiconductor Industry Association (SIA), exists.

2. Issues Related to Devices, Circuits and System Architectures

Any serious candidate for the next generation electronics should be potentially capable of surmounting the limitations of the existing technology. The present LSI is mainly based on the Boolean logic architecture which is implemented by an array of transistors which operate only as simple, small and robust switches of lumped nature. Limiting factors anticipated for this hitherto so successful technology include; (1) material and processing related limitation (doping fluctuation, avalanche break down, MOS interface instability, electromigration, stress-migration, interface reaction, etc.), (2) power limitation, (3) wiring limitation, (4) quantum mechanical limitation (quantum fluctuation, failure of device and device isolation due to tunneling), and (5) system architecture limitation.

Single electron devices (SEDs) that allow manipulation of individual electrons, are ultimate forms of the electron device. Their potential integration level is obviously extremely high due to its small size. Extremely low operation power solves some of the instability and reliability problems. The speed power product is predicted to lie close to the quantum limit set by the Heisenberg's uncertainty principle[2]. Thus, SEDs seem to be capable of overcoming some of the above limitations, if they can be operated at room temperature, and if the technology for their high density integration is made available.

Early GaAs based single electron transistors (SETs), utilizing large dots formed by split gate configuration, were based on the purely classical charging energy[3], and operated only in mK range. However, by exploiting nm-scale quantum dots which themselves behave precisely like artificial atoms[4] and molecules, various quantum effects due to quantum confinement, electron-electron interactions, tunneling, resonance etc. will be added, and they provide chances for room temperature operation as well as unexplored new possibilities for new functional devices and new architecture LSIs. Indeed, prospect of room temperature operation has been demonstrated in ultra-narrow Si wire based SETs[5,6] and metal-based SETs[7]. Room-temperature single electron memory using a ploy-Si granular structure is also being developed[8]. Use of new Schottky in-plane and wrap gate structures has also resulted in higher temperature operation of III-V based SETs[9]. Further understanding and full quantum mechanical description of electron states and transport in single and multiple quantum dots seem vitally important for future progress as well as understanding[10] and optimization[11] of single electron tunneling processes.

As for the device/system architecture of SED LSIs, one can think of the following three alternatives; (1) conventional Boolean logic based von Neumann type architecture implemented with conventional SET switch-array device architecture with improved switching performance, (2) conventional Boolean logic system architecture with a new device architecture utilizing SEDs with increased functionality than switches, and (3) non-Von Neumann architecture with new device architecture utilizing SEDs with increased functionality. One of the serious difficulty expected in the single electronics is the stochastic nature of quantum processes, and the selection or creation of the device/system architecture should be made with a serious consideration of this problem.

Quantum dot systems seem to offer unique advantages for realization of above alternatives (2) and (3). As an example, in an one-dimensional and two-dimensional arrays of dots with tunneling junctions, electrons propagate like solitons, and this may be used as wiring or to implement certain type of special information processing [12]. It has been shown theoretically that cellular automata can be constructed by chain of sets of five single electron dots [13]. Recently, binary decision device arrays [14], cellular automata and Boltzmann machine neuron arrays [15] based on more conventional tunnel junctions have also been proposed.

3. Nanofabrication Issues

For SED LSIs operating at room temperature, high density arrays of small enough dots with the sizes below 10 nm are required. Representative nanofabrication approaches include; (1) direct dot fabrication on silicon-on-insulator (SOI) wafers by Si ULSI technologies, such as EB lithography, dry etching, oxidation, etc., (2) dot formation on III-V multi layer epitaxial wafers by EB lithography and etching, (3) selective depletion of two-dimensional electron gas (2DEG) in III-V wafers by Schottky split, in-plane and wrap gates etc., (4) direct fabrication of dot nanostructures by scanned probe-induced atom-manipulation and surface reaction, (5) dot formation using the self-organizing growth mechanism in MBE or MOVPE growth of III-V materials, and (6) formation of ultra-fine particles by CVD process and various molecular reactions.

Among these, the approaches (1) and (2) are most practical if they work sufficiently well. However, process-induced damages are serious in some cases. Achievable sizes, size uniformity, size controllability and interface smoothness are also not quite sufficient yet. On the other hand, advantage of the approach (3) lies in that dots are formed far from the surface and deep in the high quality crystal in a gate controlled fashion, and that the isotropic feature of Coulomb force quickly smears the ruggedness of the surface. Weak confinement potential in the original split gate structure can be significantly increased by in-plane-gate and wrap gate geometries [9]. The approach (4) is very good for research on discrete level devices [7], but utterly impractical at present for high density integration. Examples of the approach (5) include selective growth on mesa-

patterned substrates, area-selective growth using patterned insulator windows, self-organized growth utilizing step bunching on vicinal substrates, Stranski-Krastanow (SK) mode driven self-assembly of dots, strain-driven self-organized disk formation on high-index substrates, etc. As an example, the approach (5) has led to successful realization of quantum dot-wire networks by selective MOVPE [17] and MBE [18] growth. Using the approach (6), small and uniform silicon nanoparticles have been realized with observation of Coulomb staircases at room temperature [19].

One major nanofabrication issue lies in the control of surfaces and interfaces of quantum structures. In SEDs, homo-, hetero-, MOS and Schottky interfaces control the wave-particle properties of each electron. Thus, the interfaces of SED structures should be perfect in the interface atom arrangements and be capable of producing desired potential profiles for device operation. Additionally, the interface region should be free of ionized impurities and trapping defects such as surface states, interface states and discrete deep levels. In this connection, Fermi level pinning and surface state effects have been removed recently from AlGaAs/GaAs near surface quantum wells and In AlAs/InGaAs quantum wires, using a silicon interlayer based surface passivation technique [20], opening up possibilities of insulating tunneling barriers and insulating gates on III-V materials.

Acknowledgements

The present work is supported financially in part by a Grant-in-Aid for Scientific Research Project on Priority Area of "Single Electron Devices and Their High Density Integration" (#08247101; Head Investigator, H. Hasegawa) from Ministry of Education, Science, Sports and Culture, Japan

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