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Digital Single-Electronics: Problems and Possible Solutions

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1. Introduction

The main trend in the integrated electronics for several last decades was the rapid scaling down of the typical component size. Apparently, this trend will continue for at least the next 20 years. The minimal feature size in mass-production VLSI has successfully overcome the earlier-expected limit of 1μm, and will probably cross 0.1 μm mark in not very distant future. However, the scaling down of the MOSFET technology cannot continue forever. It will hardly go beyond ~30 nm, even if adequate lithographical technology will be available. As a consequence, the search for the new principles of operation of the small-size devices is becoming more and more important.

At present there are two main branches of the proposals on the suitable operation principles: so-called "Quantum electronic devices" and "Single-electron devices". It is natural to expect that quantum effects (for example, the wave interference) will play an important role in ultrasmall electronic devices. However, fragility of the quantum effects causes the very serious doubt that they could ever be used for VLSI of the post-CMOS era. The only really robust device based on the wave interference so far is the resonant tunneling diode (RTD). However, even leaving aside the relatively large power dissipation of RTD due to finite "valley" current, we should notice that RTD is a robust device only as long as the lateral dimension is much larger than the thickness of the quantum well; decrease of the area and the transformation into quantum dot with discrete energy levels leads to common difficulties of the quantum interference devices.

In contrast to Quantum electronic devices, the *Single-electron* devices are *classical* (unavoidable quantum effects play only the secondary role). Single-electronics (for review see, e.g. Refs. [1-3]) is based on the robust effect of the electric charge discreteness which importance also increases with the size reduction. The Coulomb interaction of the single charges is used to control the correlated electron tunneling in small-capacitance structures. The main idea is quite simple. If the size and, hence, the effective capacitance C of the tunnel junction is sufficiently small, then the tunneling of only one electron produces a noticeable change e/C of the voltage across the junction. This leads to a number of effects most of which have been confirmed experimentally. Single-electron tunneling was studied using a variety of materials: metal-insulator-metal structures, GaAs quantum dots, silicon structures, large molecules with conducting cores, etc. The generality and robustness of the effect, and the relative simplicity of the device structures makes the single-electronics the most likely candidate for future ultradense digital circuits.

2. SET-transistor and pure single-electron circuits

Many proposals of single-electron memory and logic devices have been put forward (for review see, e.g. Ref. [3]). Conceptually the simplest way is to use Single-Electron Transistors (SETs) [4] instead of FETs in circuits resembling conventional electronics [5]. It is important that complementary circuits can be assembled from physically identical SET-transistors. The circuits are relatively robust in terms of the parameter margins [5], however, the maximal operation temperature is only about $0.025\ e^2/Ck_B$ where C is the capacitance of the tunnel junction, and fluctuations of the background charge should be kept within ~$0.1e$ margin. The simple logical gates can be demonstrated using present-day technology.

The drawback of this approach is the nonvanishing static current through transistors. Despite the power consumption per transistor can be very small, on the order of 10^{-9} W, it is unacceptably large for the densities above 10^{11} cm^{-2}. This problem can be circumvented in another type of single-electron logic/memory circuits which code information by the presence or absence of an extra electron on a particular conducting island. The prototype memory cells of this type have been demonstrated recently using different technologies (based on Al, GaAs, and Si - see references in [3]). Logical gates of this type are more difficult to implement because it requires the control of single electrons by single electrons and effective amplification of the signal, and so far they have not been experimentally verified.

3. Wireless Single-Electron Logic

Single-electron logic can be made "wireless" [6] with the power supplied by alternating electric field. This feature is quite important at the size scale of few nanometers. Logical functions can be realized by the specific arrangement of the small conducting islands [6] capacitively coupled due to their close location. The typical energy dissipation is on the order of e^2/C per bit processing. In the recent suggestion of Single-Electron Parametron [7] this figure is further reduced, the energy dissipation less than k_BT per switching can be achieved, that makes 3D integration possible in principal. In the proposal of Ref. [7] the rotating electric field plays simultaneously the role of the power supply and

the global clock. The non-wireless version of Single-Electron Parametron can be demonstrated using present-day aluminum technology.

4. Logic or memory?

The single-electron memory is generally much easier to implement than the single-electron logic. One of the reasons is that the operation of memory cells does not necessarily require the voltage amplification by the sensing element. As a consequence, the operation temperature of the SET-transistor in this mode can be significantly (about 5 times) higher than for similar single-electron logic circuits [8]. Moreover, the background charge independent operation [8] of SET-transistor is possible in memory applications (the idea is to pass through several periods of Coulomb oscillations during destructive read-out).

Notice that while single-electronics can be very useful for reading (sensing) the information from the small-scale memory cell, the storage element itself can be similar (just reduced in size) to the floating gate of conventional flash memories, and the Fowler-Nordheim tunneling through the barrier can be still used for writing [8] (Coulomb blockade just leads to the discreteness of the stored charge).

The concept of the background charge independent single-electron memory has been recently implemented experimentally [9] using standard aluminum technology. For real VLSI circuits the silicon technology would be obviously preferable.

Let us notice also the recent experiments [10, 11] in which the single-electron charging of the small floating gate above the narrow (10 nm wide) FET channel has been demonstrated. This type of memory can be a strong competitor for memory cells which use SET-transistors.

5. One-electron and few-electron memories

There is already a considerable number of experiments in which the storage of single electrons in different structures have been demonstrated. Such single-electron memory cells are definitely the very important experimental achievement in a sense that the number of the stored electrons cannot be further reduced. However, in author's opinion, the memory cells suitable for real applications should necessarily operate with *few* (more than one) electrons. The reason is that for one stored electron, only one erroneous event is sufficient to destroy the whole information. Hence, for DRAM the *information refreshing* will be impossible, and for the nonvolatile memory the reliability will be also quite poor. For example, even if the average retention time per cell about 10^{15} s will be achieved, the reliability of the whole device containing, say, 10^{12} memory cells will be unacceptable.

To increase reliability it is possible to use the standard methods of the information redundancy. For example, each bit can be stored by three cells. However, it is obviously much simpler to use three electrons in each cell and allow one electron to leak. The increase of the number of stored electrons improves the retention time exponentially.

In author's opinion, the optimal number of stored electrons per cell should be between 7 and 30. The further increase of this number would not only increase the power dissipation too much but would also lead to difficulties with the precise control of the number of stored electrons. (For example, the Fowler-Nordheim tunneling rate will not have sufficiently steep dependence on voltage at the single-electron scale, thus increasing the writing time).

Let us emphasize that in contrast to conventional DRAMs, the number of stored electrons in few-electron memory cells should be controlled precisely (fluctuations are due to the leakage only), so in this sense they can be still called single-electron memory cells.

6. Conclusion

There are two main obstacles on the way to practical digital single-electronics. First, this is a typically small operation temperature at present (room temperature would require few nm size scale). However, the operation of simple single-electron devices at 77K and even at room temperature has been already reported by several groups. One can hope that the necessary small-size technology will be eventually available. The second major obstacle is the sensitivity of single-electron devices to sub-electron fluctuations of the background charge induced by nearby impurities. However, even if this problem will not be solved technologically, some integrated circuits are still possible, for example, the background charge independent single-electron memory suggested in Ref. [8].

So, despite of difficulties, single-electronics has a real chance to be the basis of future ultradense integrated circuits.

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FETはSETの100万倍の集積度...