

Invited

Single-Electron Simulators for High and Low Level Analyses

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1. Introduction

Single-electron devices are promising candidates for the elements of future ultradense low power integrated circuits. The need for computer-aided analysis and design of single-electron circuits has long been recognized [1]. Low-level simulators are useful for analyzing a single device or small scale circuits with precision. For the analysis of large scale circuits, a higher-level simulator that uses simplified device models and offers high-speed simulation is required. In this article we introduce our single-electron circuit simulators: an advanced lower-level simulator and a novel higher-level simulator.

2. Low-Level Simulator — ESS

Transient Analysis Our low-level simulator, named "ESS" (Extended Single-electron Simulator), concentrate on circuits consisting of tunnel junctions, capacitors and voltage sources [2]. When a charge state is represented with a vector as $\mathbf{n} = {}^t(n_1, n_2, \dots)$, it is straightforward to obtain the following master equation [3]

$$\frac{d}{dt}P_n = \sum_m \Gamma_{nm}P_m - \sum_m \Gamma_{mn}P_n, \quad (1)$$

where Γ_{mn} is the transition rate from the state $\mathbf{n}$ to the state $\mathbf{m}$, subject to $\sum P_n(t) = 1$. Cotunneling [4] is incorporated into ESS to describe the small deviation from the semiclassical orthodox theory, utilizing the expression of Fonseca *et al.* [5]. Equation (1) can be written in a matrix form with the probability vector $\mathbf{P} = {}^t(P_n, P_m, \dots)$ and the rate matrix $\mathbf{\Gamma}$ as

$$\frac{d}{dt}\mathbf{P} = \mathbf{\Gamma}\mathbf{P}. \quad (2)$$

ESS solves the master equation using a state reduction technique similar to that proposed by Fonseca *et al.* [5]. It starts a transient simulation from a certain state specified by the user and state probabilities are iteratively calculated with Eq. (2) with dynamically resizing $\mathbf{P}$ and $\mathbf{\Gamma}$ as needed.

An Efficient Steady-State Analysis The major limitations of the Monte Carlo method are the improper handling of rare events [6] and the slow convergence. The master equation, on the other hand, can be solved only when states to be considered are determined in advance. ESS chooses necessary charge states using the Monte Carlo search [7] to traverse frequently occupied charge states and calculates state probabilities from the master equation. To search rare states, possible transition paths are tracked down recursively after the Monte Carlo search. The advantage of our new algorithm is demonstrated in Fig. 1. It shows the gate-voltage dependence of the current of a Single-Electron Transistor (SET).

Visualization of State Probabilities The solution of the master equation (2) is a set of probabilities which are usually used to calculate ensemble average of physical quantities such as voltage. An ensemble average, however, does not necessarily coincide with what is actually observed. To make it easier to grasp the behavior of a circuit intuitively, we develop a graphical tool that visualizes the probabilities of charge states, where the output is drawn so that voltages for probable states look thick and those for improbable states look thin. Figure 2

shows simulations of a three-stage ring oscillator composed of Tucker's inverters. A Monte Carlo simulation, Fig. 2 (a), predicts significant fluctuation of the oscillation frequency although the oscillation is being sustained. The average output voltage obtained by the master equation, on the other hand, quickly decays as shown in Fig. 2 (b) due to the frequency fluctuation, while the oscillation amplitude is maintained as shown in the state probabilities of Fig. 2 (c).

3. High-Level Simulator — SET-SPICE

The low-level simulator of single electron circuits requires too much computation time to simulate large scale circuits. To investigate single-electron circuits for real applications, a higher-level circuit simulator is required. We have developed a SET device model to incorporate into SPICE, named "SET-SPICE" [8]. The key strategy is to calculate node voltages from each SET's I - V characteristics and not to treat SETs as tunnel-junction networks. Besides, the incorporation of a SET device model into SPICE has no impact on other devices built into SPICE, so that SET-SPICE can simulate circuits consisting of SETs and MOSFETs. SET-SPICE can correctly handle the circuits which satisfy (i) SET is the only device that contains tunnel junctions, and (ii) all SETs are connected to circuit nodes with large capacitances to ensure small charging energy per electron except on the central nodes of SETs. I - V characteristics of a SET is calculated using the steady-state master equation where only n most probable states are considered. The state of a SET can be calculated independently of those of the other SETs in a circuit under the condition (ii). Although SET-SPICE performs simulation based on the steady-state characteristics of SETs, its transient analysis is also valid because the changes in voltage accompanying each tunneling event are small, and each SET quickly settles into a steady state under the condition (ii). As shown in Fig. 3, SET-SPICE is much faster than that solving the time-dependent master equation and the Monte Carlo simulation. Figure 4 (a) shows a test circuit for a co-simulation of SETs and MOSFETs and the simulation results are shown in Fig. 4 (b).

4. Conclusion

We have developed a low-level simulator, ESS, capable of simulating circuits of arbitrary topology consisting of tunnel junctions, capacitors and voltage sources, taking arbitrary order of cotunneling into consideration. With respect to the high-level simulation, we have introduced SET-SPICE, the SPICE circuit simulator with a SET device model. SET-SPICE performs dc analysis very fast and accurately and carries out transient simulation as well. Another advantage of SET-SPICE is its ability to simulate circuits consisting of SETs and MOSFETs. Proposed two simulators will be useful for various analyses of the integration of SETs and MOSFETs in the real-world applications.

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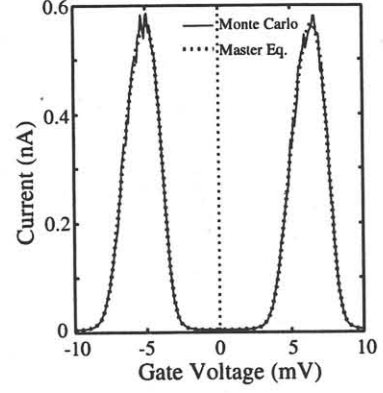


Fig.1. Gate-voltage dependence of the current of a single-electron transistor. Our new algorithm that uses the master equation in conjunction with Monte Carlo method gives accurate result (dotted line) compared to the Monte Carlo method alone (solid line). The Monte Carlo simulation is run for the duration of 1000 tunneling events. Cotunneling is taken into consideration.

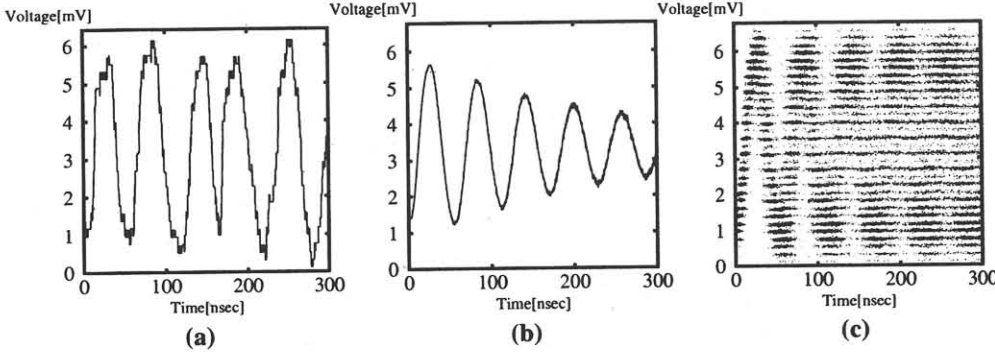


Fig.2. Simulations of a three-stage ring oscillator composed of Tucker's inverters. (a) Monte Carlo method. (b) Average output voltage. (c) Voltage distribution weighted with state probabilities. $C_1 = 1$ aF, $C_{out} = 0.36$ fF, $R_i = 5$ M Ω and $T = 0$ K. Fifteen electrons make full logic swing.

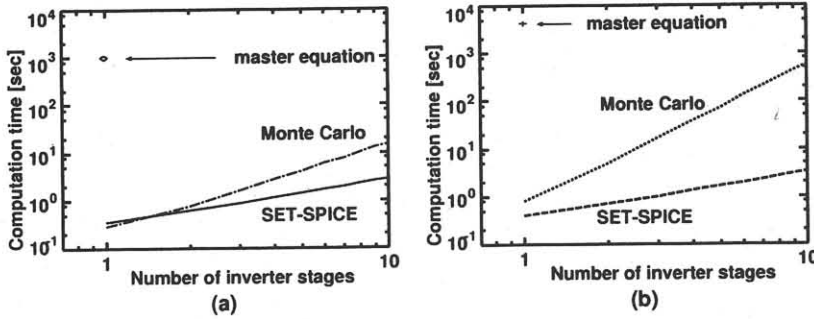


Fig.3. Computation times for simulations of an inverter chain using the master equation, Monte Carlo method (one trial) or SET-SPICE. The simulations are performed on a Sun Ultra1/170 clone. The computation time for solving the master equation for a two-stage inverter is more than 10^4 seconds. (a) Cotunneling is ignored. (b) Two-electron cotunneling is considered.

Fig.4. (a) A test circuit for a SET-MOSFET co-simulation. (b) The input and output waveforms. While the single-electron NAND gate can drive a load capacitance of only 0.2 fF at this speed, the CMOS buffer can drive no less than 10 pF. The gate capacitor of the first inverter (~ 0.19 fF) is substituted for the load capacitor connected to the output of the NAND gate. $C_L = 0.16$ fF. Gate oxide thickness $t_{ox} = 5$ nm. Threshold voltages are ± 10 mV. Mobility $\mu_p = 200$ cm²/Vs for pMOS and $\mu_n = 400$ cm²/Vs for nMOS. Inverter 1: Gate length $L = 50$ nm, gate width $W_p = 0.4$ μ m for pMOS and $W_n = 0.2$ μ m for nMOS. Inverter 2: $L = 50$ nm, $W_p = 40$ μ m and $W_n = 20$ μ m.

