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Evaluation of 0.3 μm Poly-Silicon CMOS Circuits for Intelligent Power IC Application

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1. Introduction

High voltage polysilicon device technology has been attracting interest, because polysilicon devices can be utilized as control and protection circuits for vertical power devices. Using polysilicon CMOS circuitry, formed on power devices, three dimensional system power ICs will be realized.

Currently, the development of polysilicon devices is actively made and the application target is mostly liquid-crystal displays. Low temperature fabrication process is the main concern for the display application. However, relatively high temperature process and very fine lithography can be applicable for power device applications[1][2]. In the present paper, we report the device performance of 0.3 μm gate length polysilicon CMOS fabricated on a thermal oxide film. To our knowledge, this is the first time to report the results of such fine polysilicon CMOS. The delay time of polysilicon NAND ring oscillation circuits were also measured. The results are compared with those of single crystalline CMOS circuits on SIMOX wafers. The breakdown voltage of 0.3 μm polysilicon NMOS is more than 6 V, which is greater than the breakdown voltage 3 V of 0.3 μm NMOS on SIMOX. The drain current is 540 μA, which is only a fourth of NMOS on SIMOX.

2. Experimental and Results

The schematic cross section of a n-channel polysilicon MOSFET is shown in Fig. 1. Amorphous silicon of 100 or 150 nm in thickness was deposited on thermally oxidized silicon wafers by LPCVD. The samples were annealed at 600 ℃ for 8 hrs to form polysilicon. The gate-oxide film was thermally grown at 900 ℃ in 20% HCL, and the thickness was 6 nm. The gate width was 10 μm. These devices had the LDD structure with 50 nm thick SiN-sidewall. It is noted that the used process is completely compatible with CMOS devices on SIMOX wafers. Thus, the CMOS devices on SIMOX wafers were simultaneously fabricated, using the same masks to compare the results.

Figure 2 shows the drain characteristics of 0.3 μm NMOS on 150 nm thick polysilicon. Figure 3 shows the

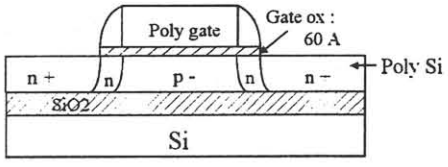

Fig. 1 Cross-sectional view of fabricated polysilicon MOSFET

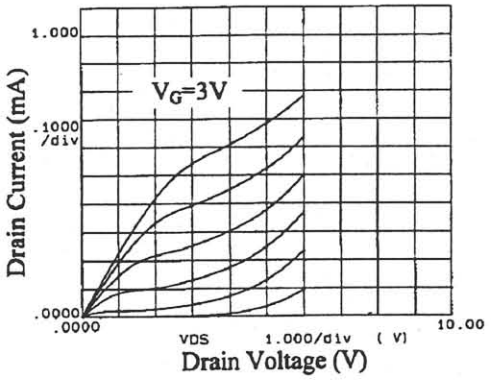

Fig. 2 Drain characteristics of 0.3 μm NMOS on 150 nm thick polysilicon

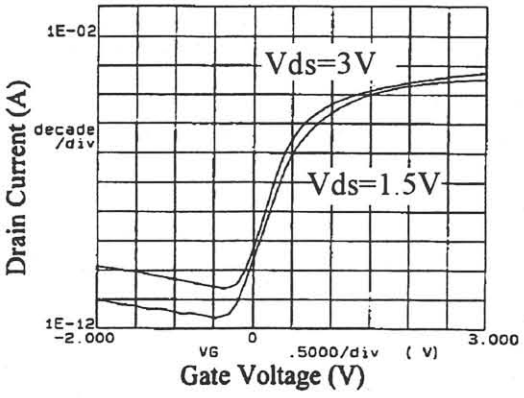

Fig. 3 Vg-logId characteristics of 0.3 μm NMOS with channel implantation

subthreshold characteristics. The breakdown voltage was increased to more than 6 V in Fig. 4, if the channel Boron implantation was carried out. If channel implantation was not made, the drain current capability was increased, the breakdown voltage was decreased and the leakage current

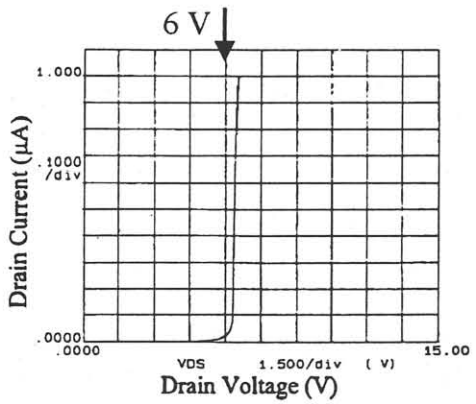

Fig. 4 Breakdown voltage of 0.3 μm NMOS on 150 nm thick polysilicon

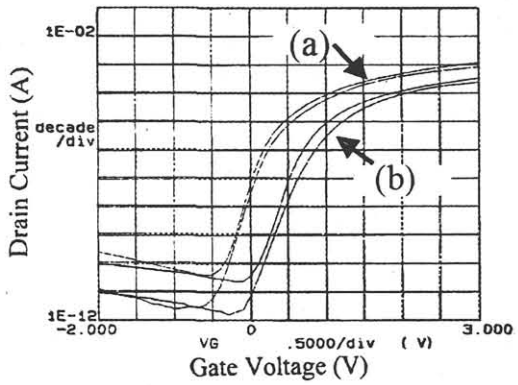

Fig. 5 Vg-Id characteristics of 0.8 μm NMOS (a) without channel implantation and (b) with channel implantation

was greatly increased when the gate voltage was zero, as shown in Fig. 5. In order to avoid the implantation damage and to increase the drain current capability (or channel mobility), it is quite effective that the channel implantation was made before the poly-crystallization annealing.

Figure 6 shows the oscillation waveforms of the fabricated ring oscillators of 0.5 μm polysilicon CMOS. The Vcc voltage was 1 V and the buffer voltage was 2 V. The number of NAND rings was fifty-one. In Fig.7, the typical NAND ring delay time characteristics are compared with the results of NAND rings fabricated on SIMOX. Because the breakdown voltage of polysilicon CMOS is greater than that of CMOS on SIMOX, a larger Vcc voltage can be applied to polysilicon CMOS rings. Thus, the short delay time of 100 ns can be achievable by polysilicon NAND rings, which is comparable to that of SIMOXs.

3. Conclusion

The present paper has analyzed the basic electrical characteristics of fine polysilicon devices for power IC application. We report the device performance of 0.3 μm gate length polysilicon CMOS. The breakdown voltage is more than 6 V, which is greater than NMOS on SIMOX.

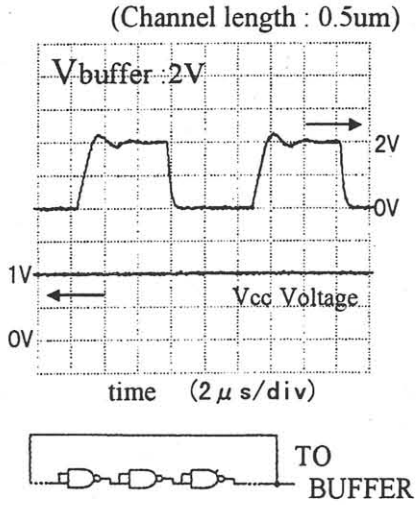

Fig. 6 Oscillation waveforms of 0.5 μm polysilicon CMOS

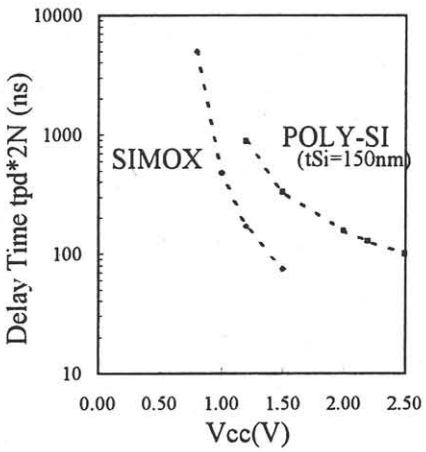

Fig. 7 NAND ring delay tima characteristics

The drain current is 540 μA, which is only a fourth of NMOS on SIMOX. The delay time of 100 nsec can be achievable by polysilicon NAND rings. It was found that 0.3 μm polysilicon CMOS is applicable to fabricate control and protection circuits on power devices.

Acknowledgment

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References

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