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Fabrication of Metal-Ferroelectric-Insulator-Semiconductor Field Effect Transistor (MEFISFET) Using Pt-$SrBi_2Ta_2O_9$-Y_2O_3-Si Structure

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1. Introduction

Ferroelectric thin films and several structures of Metal-ferroelectric-semiconductor have been intensively studied for the application of ferroelectric random access memory devices (FeRAM) [1-3]. However, one of the main drawbacks for high performance of FeRAM is how to fabricate good quality ferroelectric thin film on silicon surface because there are still so many unsolved problems such as inter-diffusion of ferroelectric and silicon, interface trap density, and charge injection to ferroelectric film [4-6]. Therefore, there is an alternative method to insert an insulator between the ferroelectric thin film and the Si [5-6]. MEtal-Ferroelectric-Insulator-Semiconductor (MEFIS) structure has been proposed as a promising method using an insulator among MgO, CeO_2, ZrO_2, and $SrTiO_3$. In this work, we have fabricated a MEFIS field effect transistor (MEFISFET) using Pt-$SrBi_2Ta_2O_9$-Y_2O_3-Si structure and investigated its electrical performances.

2. Experimental

The substrates are p-type Si (100) wafers (8~12Ω-cm). Y_2O_3 films are deposited at 35°C by rf-magnetron sputtering in Ar ambient mixed with 10% O_2 and post annealed in O_2 ambient at 600~800°C for 30mins. The thickness of Y_2O_3 is fixed at 18 nm. The $SrBi_2Ta_2O_9$ (SBT) films are prepared by Sol-Gel method on Y_2O_3/Si substrates and the post-annealing process is carried out in O_2 atmosphere at 800°C for 1 hr. The thickness of SBT is varied from 100 to 480 nm and Pt gate electrode is 500 nm. The metallurgical properties of MEFIS structures are analyzed with x-ray diffraction (XRD) and high-resolution tunneling electron microscopy (HRTEM). The MEFIS capacitors and MEFISFET's are fabricated. The area of the capacitor is $2x10^4$ μm^2 and the channel length of MEFISFET is 20μm. C-V and I-V characteristics are measured with a HP 4284A precision LCR meter and HP 4156A parameter analyzer.

3. Results and Discussion

Figure 1 shows the hysteresis in the C-V characteristic of Pt/SBT(480nm)/ Y_2O_3(18nm)/Si structure. The measurement condition is 1 MHz with 5V of applied voltage in the sweep rate of 0.2V/s. The C-V curve precedes accumulation, depletion and inversion and the hysteresis is corresponding to the memory window of MEFIS structure.

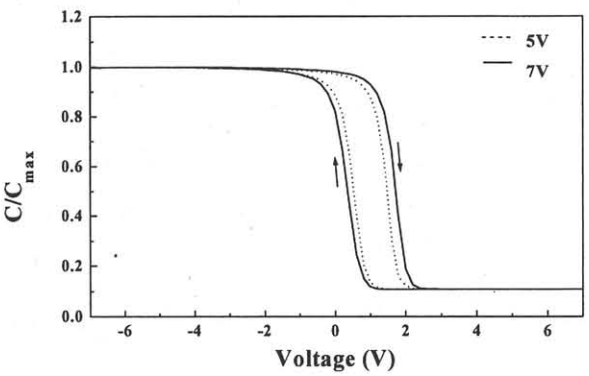

Fig. 1 C-V characteristics of SBT film on Y_2O_3/p-Si.

The memory window is 0.96V at sweep voltage of 5V and it is directly related to the voltage applied to the SBT film since the coercive electric field of the SBT film will be determined by the applied voltage. In the ideal MEFIS structure, the applied voltage is divided into the series capacitors consisted of the SBT thin film and the Y_2O_3 insulator. However, in the real MEFIS structure, SiO_2 layer grows little more during the annealing process. The applied voltage should be divided into three components; the SBT, Y_2O_3 and SiO_2 capacitors. Therefore, although the higher voltage is applied to the MEFIS structure, the voltage applied to the SBT is determined by the thickness ratio of the SBT/ Y_2O_3 while the SiO_2 thickness is fixed. Figure 2 shows the high resolution cross-sectional transmission electron spectroscopy (HRX-TEM) image for the SBT/Y_2O_3/Si structure. It shows that 4 nm thickness of SiO_2 is formed between Y_2O_3 and Si and there is no interaction at the interface that is very smooth. Therefore, increasing the applied voltage from 5 to 7V, the memory window increases to the maximum value 1.38V. However, the sweep voltage rises so high as 12 V, the memory window decreases to 0V

since charge injections take place in the SiO_2 at 12 V. Therefore, it is concluded that the maximum memory window increases with the thickness ratio of the SBT/Y_2O_3 as well as the increase of applied voltage at which the charge injection does not take place. The interface trap charge density is about 10^{11}/eV·cm², which is calculated from the C-V characteristic using the high frequency Terman method at 1MHz [1].

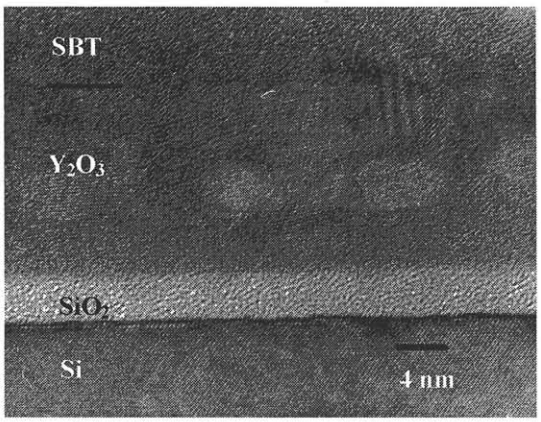

Fig. 2 High resolution cross-sectional TEM image for SBT/Y_2O_3/Si structure

Fig 3 represents the output (I_D versus V_D) characteristic of MEFISFET using the Pt/SBT(480nm)/Y_2O_3(18nm)/Si structure. The gate bias starts from 0 to 5V by 2V step. The saturation current is linearly dependent on gate voltage.

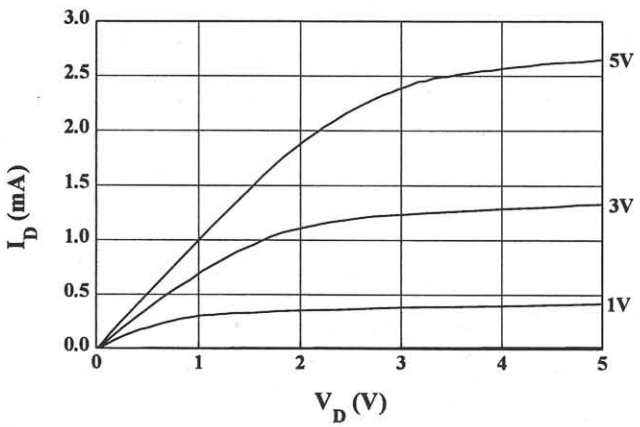

Fig. 3 I_D-V_D characteristics of MEFISFET.

Figure 4 also shows a typical transfer characteristic of MEFISFET. Note that the hysteresis in the transconductance curve indicates the memory window is 1. 4 V and the on current is 14 times the off current. The higher transconductance, higher threshold conductivity, lower power consumption, and lower leakage current. The leakage current density (not shown here) is also so low as 10^{-13} -10^{-12} A at the V_G range of 1 - 5V. Therefore, it is conclude that the electrical performances of the MEFISFET using the Pt/SBT(480nm)/Y_2O_3(18nm)/Si structure is comparable with those of the conventional MOSFET and the memory window (1-1.4 V) is higher than that of the conventional EEPROM at the lower operating of 5-7 V.

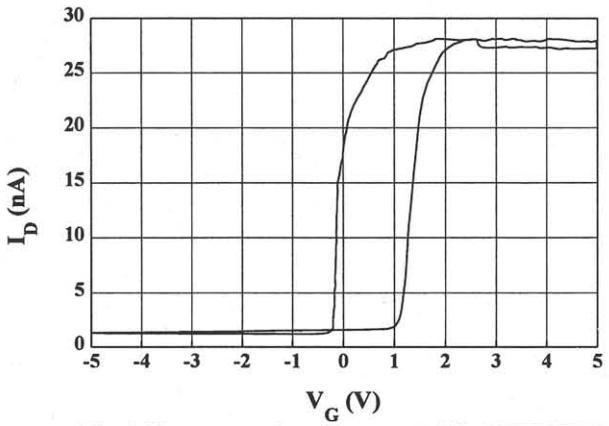

Fig. 4 The transconductance curve of the MEFISFET.

4. Conclusions

We have fabricated a MEFIS field effect transistor (MEFISFET) using the Pt-$SrBi_2Ta_2O_9$-Y_2O_3-Si structure. The memory window increases from 0.96 to 1.38V while the sweep voltage rises from 5 to 7V. The memory window of the MEFIS structure can be controlled with the variation of thickness ratio of the SBT/ Y_2O_3. The output characteristics of MEFISFET shows an excellent electrical performance compared to the conventional MOSFET and EEPROM since the memory window (1-1.38 V) is higher than the reported value of the conventional EEPROM (1 V) at lower operating voltage range of 1-7 V and the leakage current is also so low as 10^{-13} -10^{-12} A at the V_G range of 1 - 5V.

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