

An Adaptive Silicon Retina Performing an Edge Extraction with a MOS-Type Spatial Wiring and Smart Pixel Circuits

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1. Introduction

The vertebrate retina is the earliest neuronal element which performs a smart vision-processing, such as photoinput sensing, motion detection and so on. Among the retinal functions, the edge extraction of input images is the most important feature since it is believed to be necessary for the aggregation processes of the neuronal information in the brain. Recently, several artificial retina chips using silicon integration technology have been proposed for implementing the edge extraction system[1]-[5]. In those chips, a spatial smoothing task of the input images, which is performed by the retinal horizontal cells, has been realized by a resistive network[1]. The network is composed of resistive circuits which are formed by passive resistors using several MOS transistors[1]-[3] or resistors of a diffusion layer[4]. In order to improve the filtering performance of the resistive network, the pixel should be connected with not only the nearest neighbor pixels but also the second neighbor pixels[5]. However, it is very hard to connect a pixel with the second neighbor pixels since those resistive networks require a complicated wiring structure and large chip area. Our proposed silicon retina chip simplifies the wiring between pixels. Each pixel is connected to all pixels with a variable conductance, which enables the chip to adapt to global light intensities.

2. Chip Architecture

According to the biological edge-extraction mechanism, we proposed and fabricated a prototype chip which contains photoelectronic conversion (for retinal photoreceptors), the smoothing and differential calculation elements (for horizontal and bipolar cells), as shown in Fig.1. Figure 1(a) shows a top view of the chip. Each pixel is located with hexagonal layout. Figure 1(b) shows a cross-sectional view of the chip cut along the dotted line in Fig.1(a). Layout and equivalent circuits of the pixel are shown in Figs.1(c) and (d).

Each pixel corresponds to the photoreceptor and the bipolar cell, while the horizontal cell is realized with a MOS structure between the pixels. One pixel consists of two photodiodes (PD1 and PD2) and one current mirror circuit (CM). PD1 and PD2 generate the same photocurrents I_{ph} when the light is incident upon the pixel. The area between two PD2s surrounded by dotted lines in Fig.1(b) forms a pMOS transistor whose source and drain regions

are common to the p region of PD2. Thus, a spatially smoothed photocurrent I_{sm} can be obtained when I_{ph} generated in PD2 is diffused. The extent of the diffusion can be controlled by a voltage V_G which is given to the common poly-Si gate. On the other hand, I_{ph} of PD1 is independent of V_G since PD1 is isolated from PD2. Then, the output current I_{out} is obtained as a differential current between I_{ph} and I_{sm} because I_{sm} is mirrored to the output node by CM consisting of two nMOS transistors (T1 and T2).

Each pixel includes a transistor T_{sw} which acts as a switch for detecting the output current selectively. The output current I_{out} of each pixel flows out of the pixel when a control voltage V_c is given to T_{sw} . The drain of T_{sw} is common to the p region of PD1, which also makes the pixel area small.

3. Experimental Results and Discussion

The proposed retina chip shown in Fig.1 was fabricated with 10 μ m CMOS process in Toyohashi University of Technology. The chip photograph is shown in Fig.2, where 116 pixels were implemented in a 5.1mm $\times$ 5.1mm chip area.

Figure 3 shows a measured distribution of I_{out} when the light was incident upon an upper half of the chip. A white fluorescent light was used for the light source with a power density of 680 μ W/cm². The nodes were numbered along a row vertical to the edge, as shown in the figure. The edge was located between node 5 and node 6. It is shown that the edge was correctly detected by the zero-crossing output current between those nodes. Namely, large positive currents were obtained in the region where the light was applied, while large negative currents were obtained in the opposite region where no light was applied. The output currents of the pixels far from the edge were nearly zero.

In the proposed chip, a spatial resolving power is controlled by the common poly-Si gate voltage (V_G). When the input light intensity is high, the spatial resolving power can be raised by increasing V_G because I_{out} is sufficiently large near the edge. When the input intensity is low, a certain level of I_{out} can be obtained by reducing V_G at the expense of the spatial resolving power. In this way, the proposed chip could adapt to a wide range of light intensity as in the vertebrate retina.

The chip was contrived structurally to minimize a pixel area and to increase a fill factor, as explained in Fig.1. When a 0.5 μ m double-poly-Si and double-metal CMOS

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process is applied, it is estimated that the pixel occupies an area of $12\mu\text{m} \times 14\mu\text{m}$ and a fill factor is 31.4%. Then 6×10^5 pixels could be integrated in a chip with an area of $1\text{cm} \times 1\text{cm}$.

4. Conclusion

A novel silicon retina chip without complex wiring between pixels was designed and fabricated for performing the edge extraction tasks. The proposed chip has several merits in the integration process. First, all pixels are connected with a channel of MOS transistors, which simplifies the wiring structure between pixels. Secondly, each pixel consists of only two photodiodes and three MOS transistors. Thirdly, the source and drain of those transistors are common to the p region of photodiodes, which makes the pixel area small. This structure certainly increases the fill factor as well. Experimental results showed that the proposed chip performed successfully the edge extraction over a wide range of light intensity by adjusting its spatial resolution.

References

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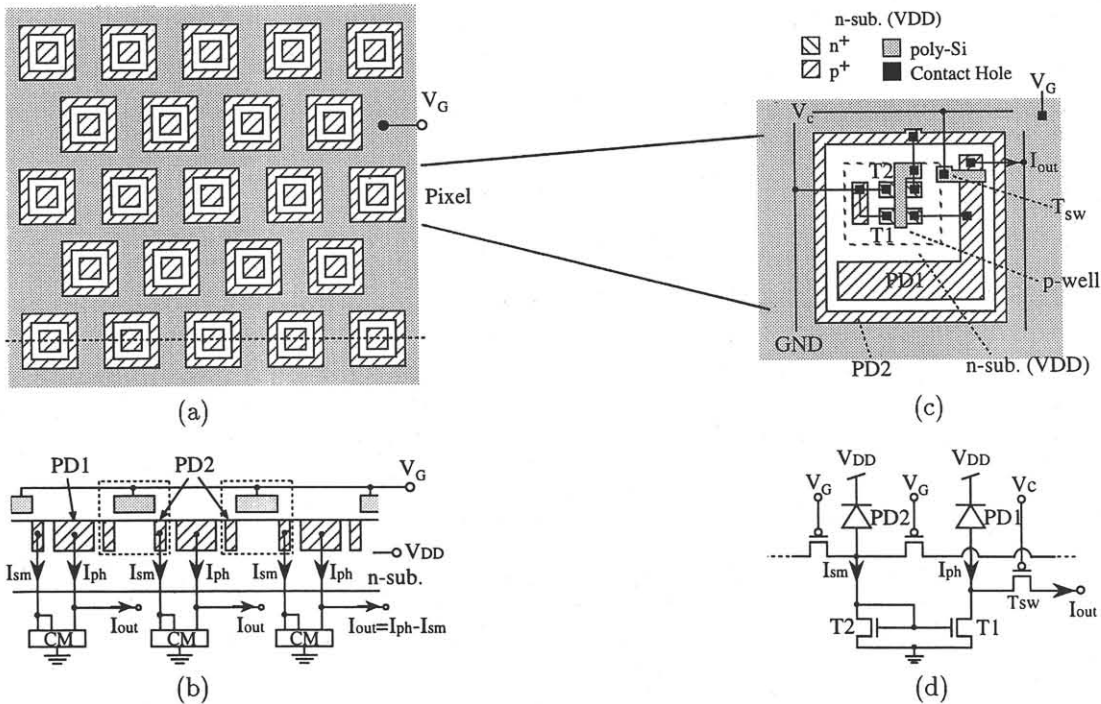


Fig.1 Structure of the proposed retina chip: (a) top view, (b) crosssectional view, (c) layout of the pixel, and (d) equivalent circuit of the pixel. Each pixel consists of two photodiodes and three MOS transistors. The area between pixels is covered with poly-Si which acts as a gate of pMOS transistors.

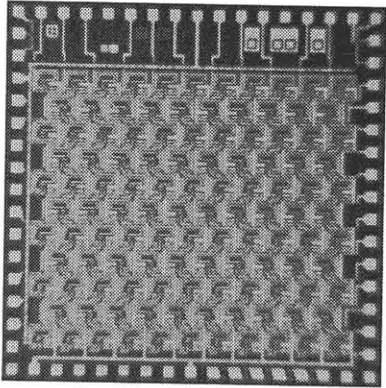


Fig.2 Photomicrograph of the fabricated chip. The chip contains 116 pixels in a $5.1\text{mm} \times 5.1\text{mm}$ chip area.

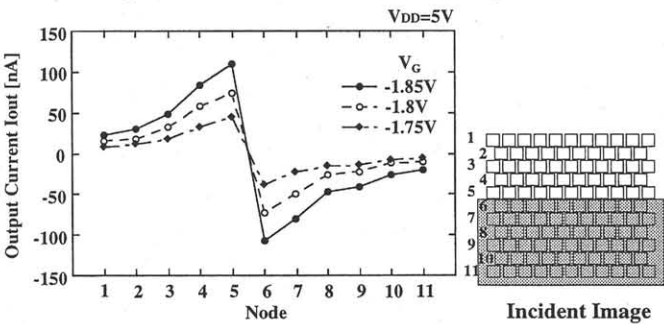


Fig.3 Measured distribution of output currents I_{out} when the light was incident upon an upper half of the chip. The nodes were numbered along a row vertical to the edge, as shown in the inserted drawing. As V_G decreased, I_{out} increased as a whole.