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Experimental Pattern Recognition System Using Bidirectional Optical Bus Lines

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1. Introduction

Recently, optical interconnections have been applied to high speed data link between racks and circuit boards. In future, they will be introduced to on-chip interconnections with the development of integration technologies of light emitting devices and waveguides, and will overcome the limitation of metal interconnections [1].
Our final target is to improve the performance of LSI systems by integrating light emitting diodes (LEDs), photodiodes (PDs), optical waveguides (WGs) and CMOS circuits on a same chip or wafer. We reported the fundamental operation of optical interconnection with the test chip which consists of optical WGs and PDs integrated on the Si wafer and CMOS chips bonded onto it [2].
In pattern recognition systems which have a number of processing units (PUs), the optical interconnection should be used not only to distribute input data and control signals, but also to communicate data between PUs. For that purpose, the bidirectional optical buses are required.
In this paper, the WGs for bidirectional optical buses are designed based on the electromagnetic analysis using a finite-difference time-domain (FDTD) method [3]. The CMOS circuits including PD amplifiers and LED drivers for the optical bus are designed and fabricated. They calculate the distances between input and reference data.

2. Pattern Recognition Processing using Optical Bus Lines

In the pattern recognition system, the global wire becomes longer and longer, as the number of PUs increases more and the pattern size becomes larger. For example, when the lengths of bus lines become over 100 mm in multi-chip-modules or wafer-scale integrated circuits, the delay time is over 10 ns for the metal wire, while it is about 1 ns for the optical interconnection [4]. This implies that optical interconnection is very effective to make a high-speed large-scale pattern recognition system.
The structure of the pattern recognition system is schematically shown in Fig. 1. The optical bus connects a number of PUs having the same function, memories for reference patterns, comparators and so on. Each unit computes the distance between an input pattern and the stored reference pattern, and the unit that has the minimum distance is selected from all the units through the optical bus. Then the reference patterns may be modified according to the matching results by a learning mechanism.
We have designed a base circuit of the system using the bidirectional optical bus. A layout of the test circuit is shown in Fig. 2. The input patterns of 4x4 pixels are matched with one of the four reference patterns in parallel. To demonstrate the advantages of optical interconnections, total length of the optical bus is set at 20 mm, and four matching circuits are connected to the bus at intervals of 5 mm.

3. Structure of Optical Bus Line

The branch structure for the bidirectional optical bus using double reflection mirrors [2] is designed by using the FDTD analysis. The electric field distributions for an optical data transmission and reception are shown in Figs. 3 (a) and (b), respectively. The incident light profile was assumed to be the TE_0 mode for simplification. Based on the branching ratio estimated under this conditions, the width at the branching point is decided and designed so that the light from any LEDs may be distributed to all PDs equably. The propagating efficiency is as high as 98~99%, but the optical power is divided at all the branching points including the branch to LED.
The waveguides are coupled with LEDs and PDs by gratings and micromirrors, respectively. The grating coupler is also used at an optical input. The layout and cross section of each coupler are shown in Fig. 4.

4. CMOS Circuit and WTA Operation

The fabricated CMOS chips consist of PD amplifiers, memories for reference patterns, exclusive ORs for comparisons, counters to calculate distances, the winner-take-all (WTA) circuits to select a minimum distance and LED drivers to send optical signals to the bus, as shown in Fig. 5.
The minimum distance is determined by comparing each bit of each distance value serially from the most significant bit. The procedure is as follows (as shown in Fig. 6) [5]:
i) If the compared bit in the own counter is "0", a unit sends the optical signal into the bus. If the bit is "1" and the light signal is sent from other units, the unit finds that the own distance is not minimum.
ii) Shifting the bit comparing to lower one, the process i) is repeated, until the least significant bit is compared.
iii) The unit left finally is the winner and has the most similar reference pattern to the input.

5. Fabrication and Measurement of Test Circuit

The test device consists of the wafer with optical bus and the CMOS chips which are bonded onto the wafer. The WGs, micromirrors, grating couplers and PDs are integrated on the wafer. Using the test device, the pattern matching operation with the optical bus will be confirmed. The micro photograph of the CMOS test chip is shown in Fig. 7. It was fabricated by the 2μm CMOS process at the Research Center for Nanodevices and Systems in Hiroshima University.
Since the optical bus is under fabrication, a principal operation for an optical input was demonstrated with a straight WGs and the CMOS test chip. The measured waveforms are shown in Fig. 8. Because of one unit operation, the signals to be received from the bus were inputted from outside. The waveforms of "Winner" represent whether the unit has the possibility of having the minimum distance ("1") or not ("0"). When "Winner" shows "1" at the 5th time step for WTA operation, it turns out that the unit has the most similar pattern to the input. Figs. 8 (a) and (b) show the waveforms for the reference patterns of "A" and "B", respectively, when the input pattern is similar to "A", showing that the circuit is operating at a clock frequency of 10 MHz. The frequency is limited by the RC time constant at the PD output node. Since it is dominantly determined by the capacitance of the bonding pad, the operation speed is drastically improved by integrating the CMOS devices and the PDs on a same chip.

6. Summary

The architecture of the pattern recognition system utilizing bidirectional optical bus was supposed. This system utilizes the optical bus to distribute input data and control signals and also to communicate between the processing units.
The waveguides for the optical bus was designed based on the FDTD analysis. The basic operations for optical inputs, distance calculations and WTAs were demonstrated at the frequency of 10 MHz with the test circuit.

References

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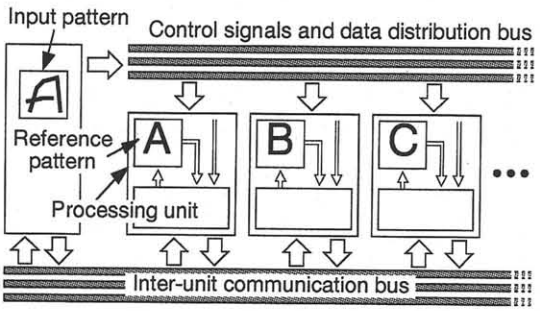


Fig. 1 Pattern recognition system using optical bus.

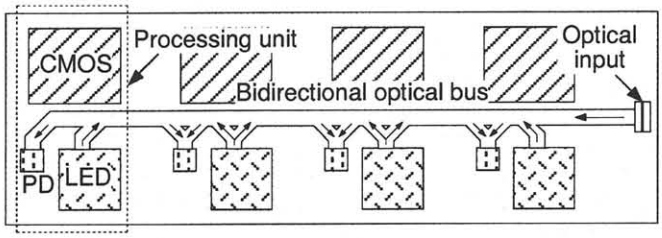
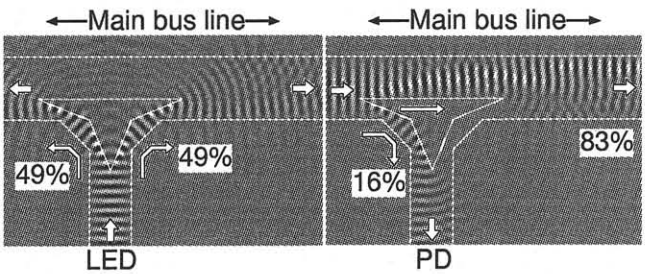


Fig. 2 Layout of pattern matching system using optical bus.



(a) Optical data transmission (b) Optical data reception

Fig. 3 Electric field in optical bus simulated by FDTD method.

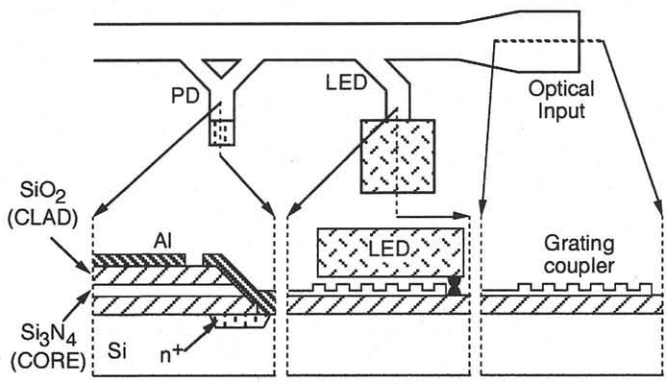


Fig. 4 Cross section of test chip.

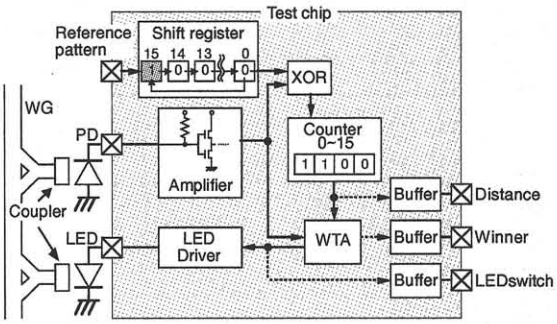


Fig. 5 Block diagram of CMOS circuit.

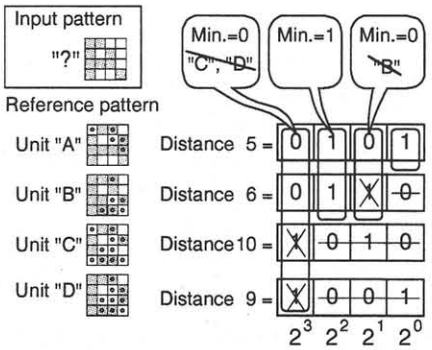


Fig. 6 WTA operation using wired OR.

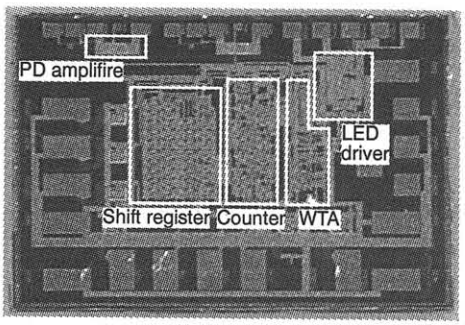
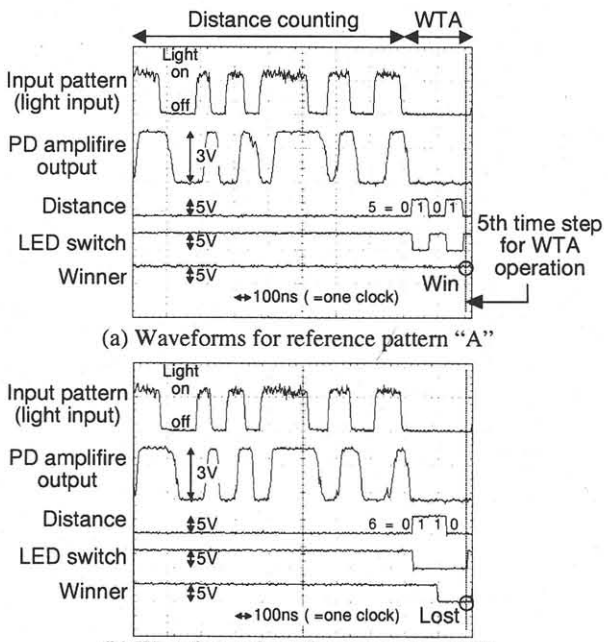


Fig. 7 Photograph of fabricated CMOS circuit.



(a) Waveforms for reference pattern "A"

(b) Waveforms for reference pattern "B"

Fig. 8 Measured waveforms.