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Deep-Submicron Single-Gate CMOS Technology Using Channel Preamorphization

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Introduction

Single-gate CMOS is still a strong candidate for high-performance scaled CMOS LSIs because of process simplicity and the high drivability of pMOS, although buried-channel (BC) pMOS is subject to short-channel effects [1]. To improve the short-channel behavior of BC pMOS, we have devised a technique for shallow boron channel doping---channel preamorphization (CP) by Si ion implantation---and have reported excellent effects on short-channel-effect suppression [2], [3]. This paper reports the application of CP to nMOS as well as to pMOS to fabricate deep-submicron single-gate CMOS. We apply CP to nMOS because sharp dopant profiles are also advantageous for nMOS [4] and show that CP improves the short-channel behavior. Utilizing CP effectively, high-performance deep-submicron single-gate CMOS with good short-channel behavior has been fabricated.

Device fabrication

The fabricated CMOS has twin-well structure with n^+ buried layers isolated by deep trenches [5]. Active regions were defined by poly buffer LOCOS [6], and then the deep trenches and retrograde wells were formed. A temporary 15-nm oxide was formed. The next step is CP: Si ion implantation was done at 150 keV and a $2x10^{15}$ cm^{-2} dose to preamorphize the surface of the channel region. This was followed by channel implantation under the conditions shown in Table 1. Recrystallization of the channel region and activation of implanted impurities were achieved by RTA at 950°C for 15 s. After etching off the temporary oxide, a 3.5-nm gate oxide was formed at 800°C. In-situ phosphorus-doped polysilicon was then deposited and deep-submicron gate patterns were defined by SR lithography and etched using RIE. Next, the gate polysilicon was oxidized slightly (20 nm). Shallow S/D extensions were formed using low-energy ion implantation: As at 10 keV to $5x10^{14}$ cm^{-2} for nMOS and BF_2 at 10 keV to $5x10^{14}$ cm^{-2} for pMOS. Preamorphization by Si ion implantation was performed for pMOS. Junction depths of S/D extensions were 50 nm for nMOS and 65 nm for pMOS. After RTA and the formation of a 100-nm SiO_2 sidewall, a relatively deep (80 nm) S/D was formed for nMOS and pMOS also using preamorphization for pMOS. Final RTA was done at 950°C for 15 s after contact ion implantation steps.

Results and discussion

(a) Effects of CP on nMOS

Fig. 1 shows electrically active boron depth profiles in the channel region for nMOS measured by the pulsed MOS C-V method. Boron was implanted at 35 keV to $2.5x10^{12}$ cm^{-2} for these devices. It can be seen that the boron profile is sharper for devices with CP. This is because CP suppresses transient enhanced diffusion (TED) during annealing as well as channeling during ion implantation [2]. Fig. 2 shows the effects of CP on the V_{th} roll-off characteristics of nMOS. V_{th} for long-channel devices is slightly lowered by CP because the surface boron concentration is lowered. It can be seen that short-channel effects are suppressed for nMOS with CP, and that reverse short-channel effects (RSE), which are observed for nMOS without CP, are also suppressed. The effect of CP on short-channel behavior improvement can be clearly seen in Fig. 3, which shows saturated transconductance as a function of ΔV_{th}(DIBL) at V_D=2V. The short-channel behavior improvement is due to the sharper retrograded boron profile [4] obtained by CP. The origin of RSE is considered to be profile broadening of channel dopant (boron) due to enhanced diffusion arising from S/D implantation or reoxidation process [7]. Fig. 4 shows the increase in V_{th} due to channel boron profile broadening for long channel devices calculated by process and device simulation. In this figure, V_{th} is shown as a function of Dt (diffusion coefficient x time). It can be seen that the increase in calculated V_{th} due to profile broadening is larger for devices with CP. This means that RSE should be more pronounced for devices with CP, contrary to the experimental results. RSE suppression is, therefore, attributed to some effect of CP that suppresses the enhanced diffusion causing RSE.

(b) Electrical characteristics of fabricated deep submicron CMOS

Fig. 5 shows (a) I_D-V_D characteristics and (b) subthreshold characteristics of 0.1-μm-gate-length nMOS. The 0.1-μm nMOS shows long-channel behavior. Fig. 6 shows the dependence of V_{th} on gate length, and Fig. 7 shows the dependence of saturated transconductance g_{mmax} on gate length, for both nMOS and pMOS. As is apparent from these results, high-performance deep submicron nMOS and pMOS have been fabricated. The measured gate delay of a 53-stage unloaded CMOS ring oscillator, which consists of 0.1-μm-gate-length nMOS and 0.13-μm-gate-length pMOS, is shown in Fig. 8 as a function of V_{DD}. The gate delay is 17.1 ps at 1.5 V, and 14.8 ps at 2 V. These values are small considering that no silicidation process was used. Thus, high-performance deep submicron CMOS has been fabricated using CP.

Summary

Deep-submicron single-gate CMOS technology using CP was described. CP improves the short-channel behavior of nMOS as well as pMOS because sharp and shallow boron channel doping is achieved. CP also suppresses RSE in nMOS. Utilizing CP effectively, deep-submicron single-gate CMOS with good short-channel behavior has been fabricated.

Acknowledgment

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Table 1 Ion implantation conditions for channel doping

nMOS	B, 25 keV, 5.0E12cm-2 B, 70 keV, 7.6E12cm-2
pMOS	BF2, 25 keV, 1.35E13 cm-2 As, 130 keV, 6.0E12 cm-2 P, 170keV, 3.2E12 cm-2

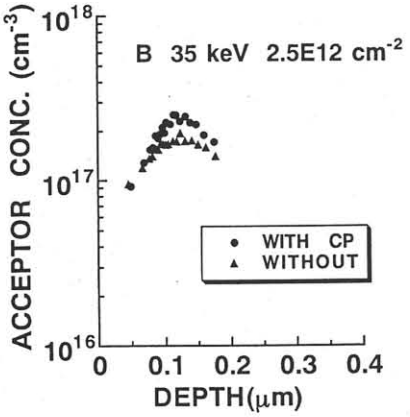


Fig.1 Electrically active boron depth profiles in the channel region for nMOS.

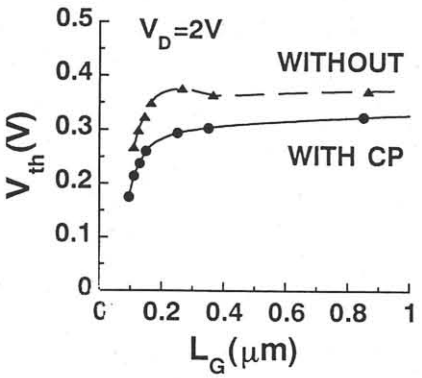


Fig.2 Effects of CP on roll-off characteristics of Vth for nMOS.

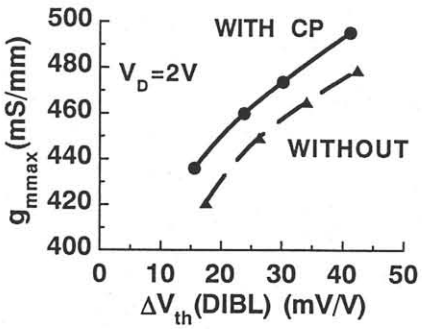


Fig.3 Saturated transconductance as a function of ΔVth(DIBL) for nMOS.

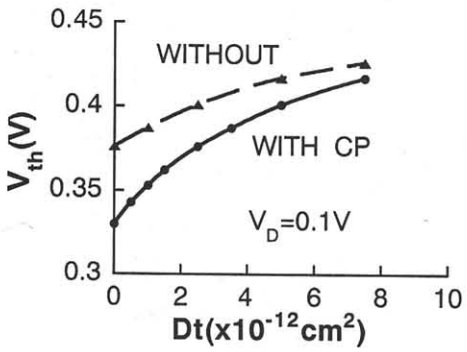
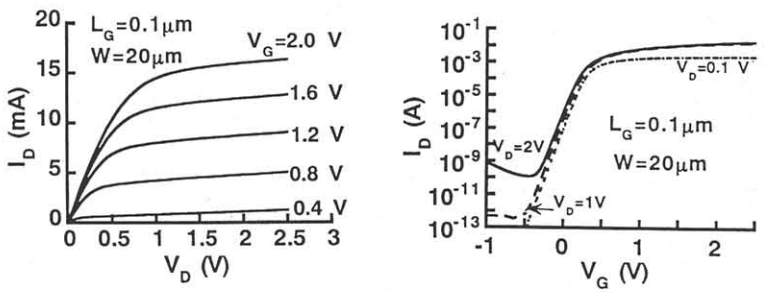


Fig.4 Increase in Vth due to profile broadening calculated by process and device simulation.



(a) (b)

Fig.5 (a) ID-VD characteristics and (b) subthreshold characteristics of 0.1-μm-gate-length nMOS.

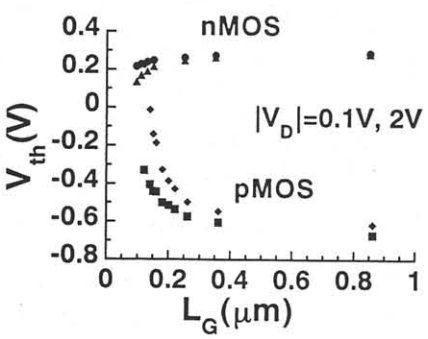


Fig.6 Dependence of Vth on LG for both nMOS and pMOS.

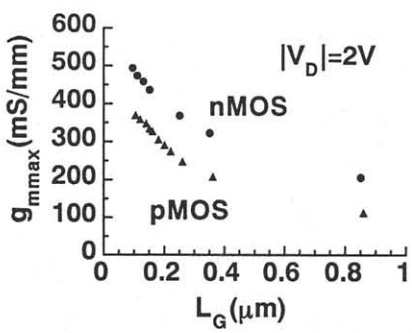


Fig.7 Saturated transconductance as a function of LG for both nMOS and pMOS.

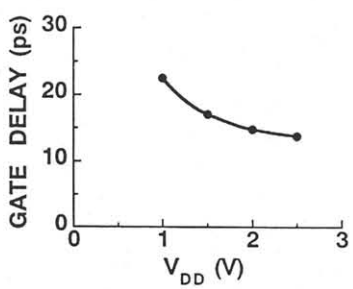


Fig.8 Gate delay as a function of VDD for deep submicron CMOS ring oscillator.