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Impact of Shallow Source/Drain on Scaling pMOSFETs below 0.1 μm

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1. Introduction

Reducing the source/drain (S/D) junction depth X_j is considered to be an effective way to suppress short channel effects for scaling MOSFETs to smaller sizes [1]. However, reductions in X_j lead to a longer effective channel length L_{eff}. The two parameters X_j and L_{eff} are not independent. Although some simulation results indicate a weak impact of X_j in suppressing the short channel effect [2], it has not been experimentally clarified which parameter affects short channel characteristics more seriously. In this paper, we examined this issue by analyzing the effect of X_j and L_{eff} when scaling pMOSFETs below 0.1 μm.

2. Fabrication and Analysis of pMOSFETs

We need to precisely determine X_j and L_{eff} to analyze the impact of these two parameters on the short channel characteristics. To obtain a shallow X_j, we fabricated pMOSFETs using solid phase diffusion (SPD) from a boro-silicate glass (BSG) sidewall, because the SPD process is free from the complexities caused by transient enhanced diffusion. We fabricated three pMOSFETs with the structure shown in Fig. 1. These are different only in the process conditions for SPD that are summarized in Table I. We obtained S/D extension profiles with different X_j's as shown in Fig. 2.

To extract L_{eff} precisely, we modified the Shift & Ratio (S&R) method. Although the original S&R method assumes a constant parasitic resistance R_{sd} [3], we considered the dependence of R_{sd} on the gate voltage. We analytically modeled the total resistance of a short channel MOSFET as

$$R_i=\frac{L_i}{W}R_{ch}(V_g-V_{th})+\frac{L_{sd}}{W}R_{sd}(V_g-V_{th})+R_{sd} \quad (1)$$

while modeling the long channel MOSFET as usual. The first term in Eq.(1) represents the intrinsic channel resistance in which L_i denotes the intrinsic channel length. The second term represents the parasitic S/D resistance, which depends on the gate voltage. It is modeled as a MOSFET with a channel length of L_{sd} connected in series with the intrinsic channel. The third term is the parasitic S/D resistance, which is independent of the gate voltage. We take the ratio (r_i) of the total resistance between a short channel MOSFET and a long channel (reference) MOSFET and determine the difference in gate voltage to minimize the mean square deviation of r_i. Then we can obtain L_{eff} dependent on V_g as

$$L_{eff}(V_g)=r_iL_0=L_i+L_{sd}\cdot f(V_g) \quad (2)$$

where $f(V_g)$ is a gate voltage-dependent function described as the ratio between $dR_{sd}(V_g-V_{th}^-)/dV_g$ and $dR_{ch}(V_g-V_{th}^o)/dV_g$ where $R_{ch}(V_g-V_{th}^o)$ is the channel resistance of a long channel MOSFET. By using this $L_{eff}(V_g)$, we can obtain the parasitic $R_{sd}(V_g)$ that is dependent on V_g. An example of an extracted $L_{eff}(V_g)$ and $R_{sd}(V_g)$ in pMOSFETs with a gate polysilicon length (L_{poly}) of 0.2 μm is shown in Figs. 3 and 4, respectively. The extracted L_{eff} is shorter in the sample with a larger X_j. The L_{eff} in sample A shows a stronger dependence on gate voltage, because L_{eff} is modulated in a sample with a lightly doped S/D extension [4]. The extracted R_{sd} is largest in sample A, and the gate voltage dependence of R_{sd} is also strongest in sample A.

3. Discussion

Figure 5 shows the threshold voltage (V_{th}) for a drain voltage of V_d=-2 V versus gate polysilicon length (L_{poly}) measured by SEM. V_{th} is defined as V_g for a constant drain current of I_d=0.1 μA/μm. The V_{th} roll-off is smaller in a sample with a shallow X_j. However, Fig. 6, in which the same data is plotted versus L_{eff}, shows that V_{th} is plotted universally on a single curve regardless of X_j. Similar behavior was obtained when we plotted the change in V_{th} caused by drain induced barrier lowering versus L_{poly} and L_{eff}. Hence, a difference in X_j does not affect the short channel effect in MOSFETs with the same L_{eff}. The short channel effect is determined by the shrinkage of L_{eff} which accompanies a deep X_j.

In Fig. 7, we showed the saturation drain current I_{dsat} for the same gate overdrive (V_g-V_{th}) versus L_{eff}. The higher current drivability in sample B is attributed to a lower R_{sd}, because the carrier density in the channel and the L_{eff} are the same for both samples in this figure. In Fig. 8 we compared the I_{dsat}-I_{off} characteristics of our samples with the published data for short channel pMOSFETs [5, 6]. The device characteristics of sample B for the shorter L_{eff}, which corresponds to a higher I_{dsat}, is comparable to the best ever reported. The improved current drivability in these short channel devices is attributed to the reduced R_{sd}.

4. Conclusion

We experimentally showed that a shallow X_j does not improve the performance of ultra-small pMOSFETs, as long as the surface impurity concentration at the S/D extension is low. The short channel effect is almost the same for MOSFETs with the same L_{eff}, if we compare devices having a different X_j. The current drivability is higher in devices with a deeper X_j because of a reduced R_{sd}. Hence, there is no merit in a device process which achieves a shallow X_j by decreasing the surface impurity concentration.

Acknowledgements

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References

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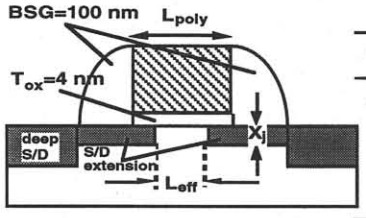

Table I Fabrication conditions for S/D extnsion by SPD.

Sample	Boron in BSG	RTA	X_j (@1×10^{18}cm^{-3})
A	10 mol%	1000°C, 10 s	25 nm
B	15 mol%	1000°C, 5 s	55 nm
C	20 mol%	950°C, 10 s	70 nm

Fig. 1 Schematic of pMOSFET using SPD.

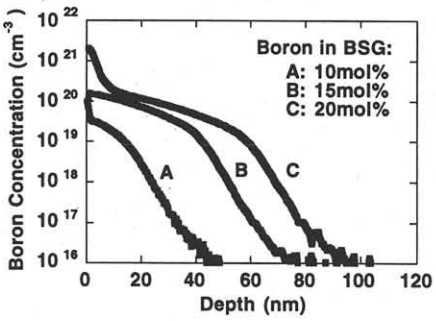

Fig. 2 SIMS profile of boron for S/D extension formed by SPD.

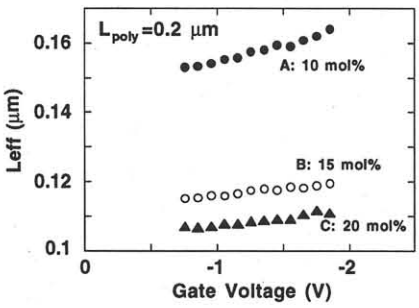

Fig. 3 Gate voltage dependence of effective channel length L_{eff} for three samples A, B, and C. Gate polysilicon length L_{poly} is 0.2 μm.

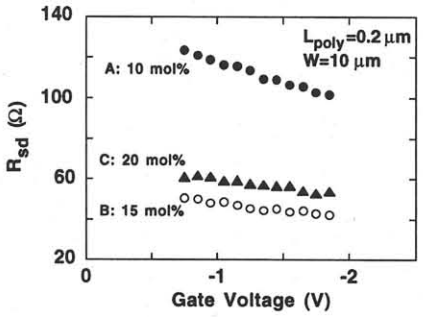

Fig. 4 Gate voltage dependence of parasitic S/D resistance R_{sd} corresponding to Fig. 3. R_{sd} in sample C is higher than sample B because of RTA temperature.

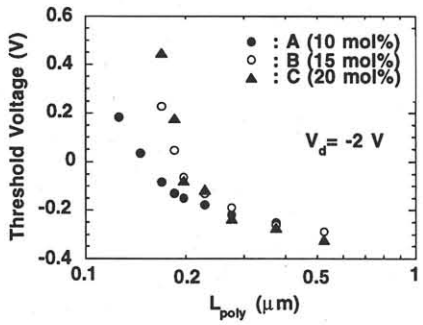

Fig. 5 Threshold voltage versus gate polysilicon length measured by SEM.

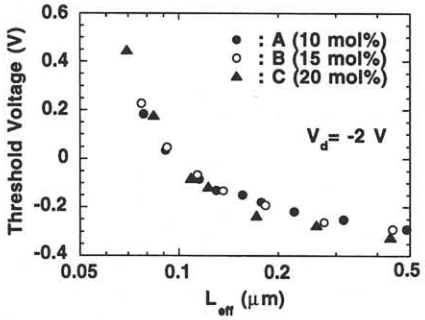

Fig. 6 Threshold voltage versus effective channel length extracted by modified S&R method.

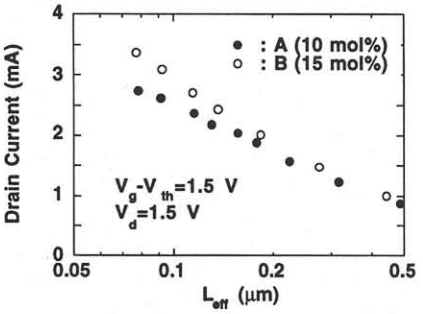

Fig. 7 Drain current for same gate overdrive V_g-V_{th}=1.5 V plotted versus effective channel length. Gate width is 10 μm.

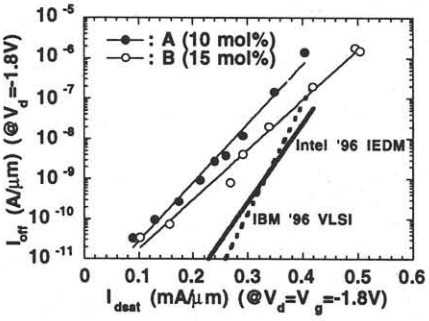

Fig. 8 Saturation drain current I_{dsat} versus off current I_{off} in samples A and B compared with published data.