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A New Post-Metal Threshold Voltage Adjustment Scheme by Hydrogen Ion Implantation

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1. Introduction

For high-end or low-power CMOS devices, an accurate control of threshold voltage is crucial. In conventional process, V_{th} is determined by channel doping that is performed early in the fabrication process, and cannot be corrected afterwards even if a variation in device parameters such as gate length and gate oxide thickness is large. With scaling down of device sizes, an accurate control of V_{th} becomes more difficult because of higher susceptibility of V_{th} on the process variation.

This paper proposes a new feed-forward adjustment scheme of V_{th} by using post-metal hydrogen ion implantation. We have found that implanted hydrogen deactivates channel impurities and decreases V_{th}, and that this effect remains stable after a normal post-metalization anneal (400 °C). This effect is different from the previously reported effect [1], which is stable only below 200 °C. Using this technology, the V_{th} can be adjusted at the metalization step after measuring the actual value (Fig. 1).

2. Experimental

NMOS and PMOS FETs were used in this study (Fig. 2). The gate structure consisted of a 6.4-nm-thick gate oxide layer and 0.2-μm-thick layer of polysilicon. The minimum gate length we evaluated was 0.2 μm, and a Ti-salicide process was used. After interlayer dielectrics with 0.15-μm-thick SiO_2 and 0.45-μm-thick BPSG were deposited and planarized by CMP, a metal interconnect was formed. Hydrogen ions were implanted, with energies of 50 – 150 keV, into the channel region through the dielectrics and gate electrode at dosages of $1 \times 10^{12} - 1 \times 10^{15}$ cm^{-2}. Both implanted and unimplanted (reference) samples were annealed in forming gas (50 % H_2, 50 % N_2) at 400 °C for 20 min. Transistor characteristics and oxide reliability were evaluated.

3. Results and Discussion

With an increase in the H^+ dosage, $|V_{th}|$ became smaller in both NMOS and PMOS FETs (Fig. 3). The obtained V_{th} shift was 0.1 V at 1×10^{13} cm^{-2} and 0.45 V at 1×10^{15} cm^{-2} for NMOSFET. The I_d-V_g characteristics in Fig. 4 show that H^+ implantation at dosages $< 1 \times 10^{14}$ cm^{-2} slightly decreased the subthreshold slope. This improvement is due to a reduced channel doping density. The implanted H^+ ions might also have decreased the subthreshold slope by passivating the interface states. When the H^+ dosage was increased to 1×10^{15} cm^{-2}, subthreshold slope increased significantly because oxide damage caused by the implantation could not be fully removed by a post-metal forming gas anneal at 400 °C. Although H^+ implantation increased the off-leakage current, this increase is small for practical usage. Also note that since V_{th} can only be decreased by this technology, V_{th} needs to be set, in advance, slightly larger than the desired value.

The V_{th} shift was most effective at 75 – 100 keV. As confirmed by the SIMS depth profile (Fig. 5), this corresponds to the energy at which the hydrogen concentration has its peak near the gate oxide. The H^+ implantation also enhanced the short channel effect (Fig. 6), which is due to a decrease in channel impurity density. This is also obvious from the backgate characteristics shown in Fig. 7.

There are many reports about the impurity deactivation effect caused by atomic hydrogen [1]. They say that the impurity deactivation is due to the formation of a hydrogen-impurity complex (only with an acceptor impurity), and that this complex is not thermally stable above 200 °C. Our results cannot be explained by this mechanism. One possibility is that not only the implanted H^+ but also Si interstitial defects are related to the deactivation effect.

A major concern of this technology is its impact on device reliability, since devices can be annealed only at low temperature (≤ 400 °C) after the H^+ implantation. Although several adverse effects were observed, they were found to be small for practical usage for H^+ dose $< 1 \times 10^{14}$ cm^{-2}.

H^+ implanted junction showed a larger leakage current (Fig. 8) because of the Si lattice damage caused by the implantation. However, the effect of this leakage current on the device characteristics is small (Fig. 4). Charge-to-breakdown (Q_{bd}) showed a negligible decrease for H^+ dosages up to 1×10^{13} cm^{-2}, and a slight decrease for 1×10^{14} cm^{-2} (Fig. 9). Although at 1×10^{15} cm^{-2}, Q_{bd} decreased to 10 Ccm^{-2}, the oxide breakdown voltage was the same as the reference (Fig. 10). The hot carrier lifetime of H^+-implanted samples (1×10^{14} cm^{-2}) was about 1/10 of that of the reference (Fig. 11) due to interface damage by the implantation.

4. Conclusion

We have demonstrated a new threshold voltage adjustment technology using post-metal hydrogen ion implantation. This technology makes it possible to compensate the V_{th} deviation due to process fluctuation, and enables controlling the V_{th} after the metalization process. This H^+ implantation technique has significant potential for VLSI device fabrication.

Reference

[1] C.-T. Sah, J. Y.-C. Sun, and J. J.-T. Tzou: Appl. Phys. Lett. **43** (1983) 204.

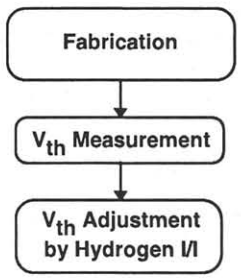


Fig. 1. V_{th} adjustment scheme by using H^+ implantation.

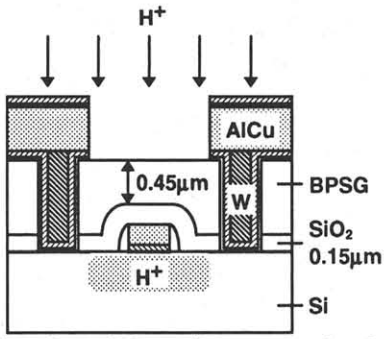
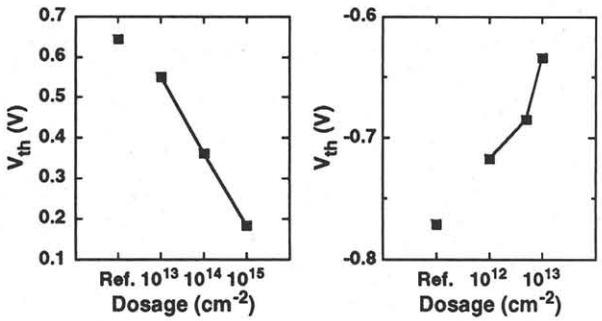
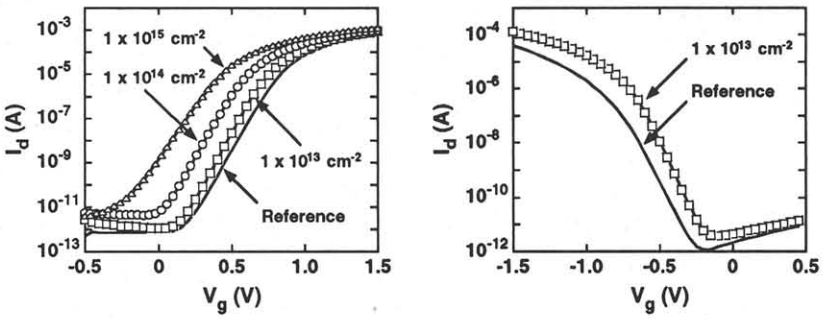


Fig. 2. Schematic cross-sectional view of a MOSFET. The gate width is 10 μm. The minimum gate length is 0.2 μm. The gate polysilicon thickness is 0.2 μm, and the gate oxide thickness is 6.4 nm.



(a) NMOS (b) PMOS

Fig. 3. The dependence of threshold voltage on hydrogen ion dosage (75-keV implantation, V_{th} at V_d=2.5 V, I_d=0.2μA).



(a) NMOS (b) PMOS

Fig. 4. Subthreshold characteristics of a H^+-implanted MOSFET (100-keV implantation, L_{gate}=0.32 μm, I_d at V_d=2.5V).

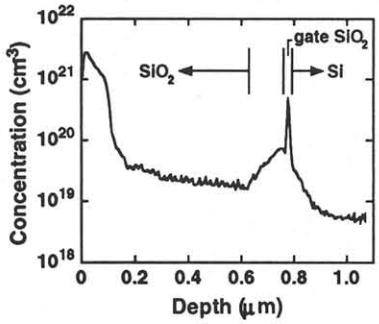
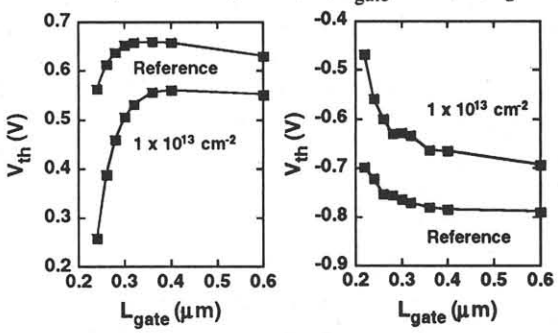


Fig. 5. Hydrogen depth profile obtained by SIMS (1 x 10^{15} cm^{-2}, 75 keV). The sharp peak at the gate oxide is an artifact caused by the calculation of hydrogen concentration.



(a) NMOS (b) PMOS

Fig. 6. Dependence of threshold voltage on gate length (100-keV implantation, V_{th} at V_d=2.5 V, I_d=0.2 μA).

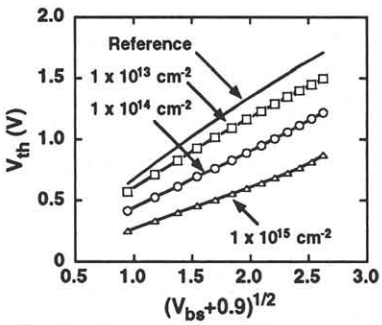


Fig. 7. Dependence of V_{th} on backgate bias (75-keV implantation).

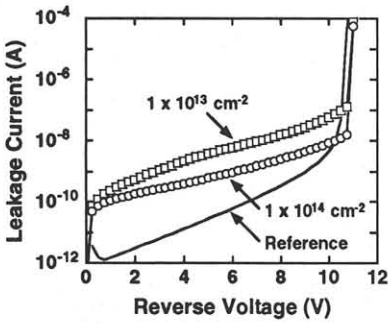


Fig. 8. Junction leakage current of 500 μm x 500 μm N^+/P junction (100-keV implantation).

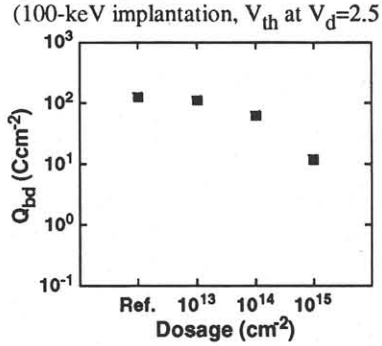


Fig. 9. Dependence of charge-to-breakdown of MOSFET on hydrogen ion dosage (75-keV implantation, stress current =0.5 Acm^{-2}, at 300 K).

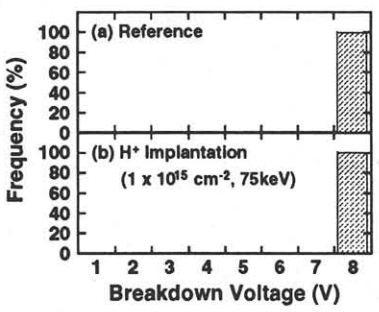


Fig. 10. Oxide breakdown voltage of MOSFET.

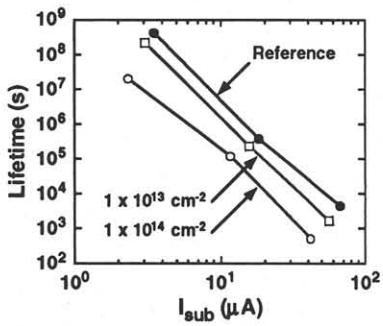


Fig. 11. Hot carrier lifetime of MOSFET under drain avalanche hot carrier injection (lifetime was defined as the time for 10 % degradation of I_d, stressed at V_g of I_{submax}, I_d was measured at V_d=V_g=2.5 V).