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High Performance 0.2 μm Dual Gate CMOS by Suppression of Transient-Enhanced-Diffusion Using Rapid Thermal Annealing Technologies

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1. INTRODUCTION

Super steep retrograde (SSR) channel profile formed by implantation using heavy ion such as Sb or In is promising to reduce threshold voltage with suppressing punch-through phenomena [1]. It is, however, important to suppress transient-enhanced-diffusion (TED) in order to realize steep profile even in the use of conventional dopant ions such as B, As and P. It has been reported that the dominant diffusion mechanism changes from thermal diffusion to TED around 800 °C wafer process for 0.2 μm regime [2]. Since radiation damage induced by ion implantation causes to promote TED during low temperature process around 700-800 °C, elimination of the implantation damage is useful to suppress TED and to keep the implanted profile steep.

Rapid thermal annealing (RTA) process is one of the adequate solution against TED. RTA before gate oxidation was reported to make channel profile more abrupt [3, 4]. RTA before TEOS deposition for sidewall spacer was reported to suppress spreading p^- extension profile [5]. Above-mentioned reports treated with only B diffusion.

In this paper, TED suppression of As and P besides B by RTA process has been systematically investigated using experiments and simulation based on point defect diffusion. The combination of RTA processes before gate oxidation and before TEOS deposition for sidewall spacer was applied to 0.2 μm dual gate CMOS for improvement of current drivability.

2. EXPERIMENTAL

Fig. 1 shows fabrication steps and conditions for 0.2 μm dual gate CMOS in this experiment. In the nMOSs, B was implanted into the channel for threshold voltage adjustment, and As and P were implanted into the S/D extensions. In the case of pMOSs, two kinds of channels were formed with As and P implantation, and S/D extension was formed with BF_2 implantation. RTA ranging from 800 to 1100 °C for 30 seconds in N_2 ambient was additionally introduced before 50 Å wet-gate-oxidation at about 750 °C. RTA was also added before TEOS deposition at about 700°C for formation of sidewall spacer. Finally, S/D was drived at 800°C. Moreover, the final channel profiles were simulated using point defect based diffusion model for clarification of TED suppression by RTA [6, 7].

3. RESULTS AND DISCUSSION

RTA before gate oxidation

The dependence of extrapolated threshold voltage (Vthe), drain current at 2V supply (Ids), sub-threshold swing (SS) and transconductance (g_m) of 0.22 μm transistor upon temperature of RTA before gate oxidation is depicted in Fig. 2. Figs. 2 (a) , (b) and (c) show nMOS with B-channel, pMOS with As-channel and pMOS with P-channel, respectively. Vthe decreases with increase in RTA temperature. In particular, Vthe drastically reduces in the cases of B and P-channel, which indicates that RTA treatment suppresses TED, so that channel concentration at the surface is reduced. RTA is thought to be capable to eliminate great deal of point defects induced by channel ion implantation. The increase in Ids is caused by the decrease in Vthe and the increase in g_m. The g_m increases by 10% in nMOS with B-channel. SS of the samples treated by RTA is almost the same as that without RTA. Therefore, RTA treatment does not deteriorate punch-through characteristics, thereby subthreshold leakage current (Ioff) maintains regardless of RTA process. In the case of pMOS with As-channel, Vthe changes slightly with increase in the temperature of RTA. This fact concludes that TED of As is not more remarkable than those of P and B.

Simulation

Fig. 3 compares the final channel profiles simulated by point defect based diffusion model. B, As and P channel profiles in Figs. 3 (a), (b) and (c) correspond to the channel profiles in Figs. 2 (a), (b) and (c), respectively. The simulated profiles are in good agreement with the tendency of Vthe in Fig. 2. The B profile treated by RTA at 1000 °C is the most abrupt, so that the Vth calculated from the simulated profile is the lowest among all the RTA conditions. While P profiles become slightly abrupt by RTA, As profiles scarcely change by RTA. The effects of TED suppression by RTA are listed as follow : B > P > As. The simulated channel concentration at the surface in the sample treated by RTA at 1100 °C is higher than that at 1000 °C due to predominant thermal diffusion.

RTA before sidewall spacer TEOS deposition

The dependence of short channel characteristics of the threshold voltage lowering upon RTA temperature before TEOS deposition for sidewall spacer is shown in Fig. 4. RTA is expected to suppress TED of S/D extension. Figs. 4 (a) and (b) exhibit the cases of nMOS with P-extension and pMOS with BF_2-extension, respectively. The Vth lowering in both cases is improved by RTA due to TED suppression in the lateral and vertical regions of the implanted extension. It should be noted that RTA at 900 °C is the most effective to improve the short channel effect.

Ids-Ioff characteristics

Fig. 5 shows Ids-Ioff characteristics between the samples with conventional process and the ones treated by RTA processes before gate oxidation and before sidewall spacer TEOS deposition. Figs. 5 (a) and (b) correspond to nMOS with B-channel and P-extension, and pMOS with P-channel and BF_2-extension, respectively. Since RTA treatment can decrease Vth, increase g_m and suppress Vth lowering, Ids-Ioff characteristics are to be improved.

4. CONCLUSIONS

RTA processes have been introduced into 0.2 μm dual gate CMOS process to suppress TED. Consequently, current drivability can be improved by the elimination of TED to channel and extension impurities using the combination of RTA treatments before gate oxidation and before TEOS deposition for sidewall spacer. It was found that RTA just before low temperature process ranging from 700 to 800 °C can suppress TED of B and P, and that the optimum conditions are 900-1100 °C for RTA before gate oxidation and 900 °C for RTA before sidewall spacer TEOS deposition to suppress both TED and thermal diffusion.

References

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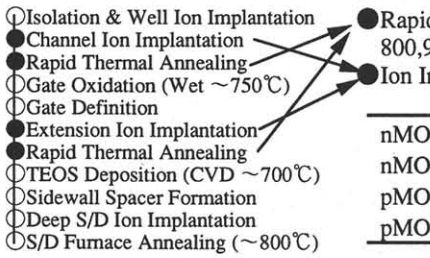

Rapid Thermal Annealing
800,900,1000,1100℃ 30seconds in N_2 ambient
Ion Implantation Conditions

	Channel	Extension
nMOS1	B 50keV $1.6\times10^{13}cm^{-2}$	As 30keV $2.8\times10^{13}cm^{-2}$
nMOS2	B 50keV $1.6\times10^{13}cm^{-2}$	P 10keV $1.0\times10^{13}cm^{-2}$
pMOS1	As 200keV $1.6\times10^{13}cm^{-2}$	BF_2 10keV $1.0\times10^{14}cm^{-2}$
pMOS2	P 140keV $1.6\times10^{13}cm^{-2}$	BF_2 10keV $1.0\times10^{14}cm^{-2}$

Fig.1 Fabrication steps and conditions for this experiment. Ion species for channel and extension implantations and temperature of RTA are changed to investigate effect of transient-enhanced-diffusion.

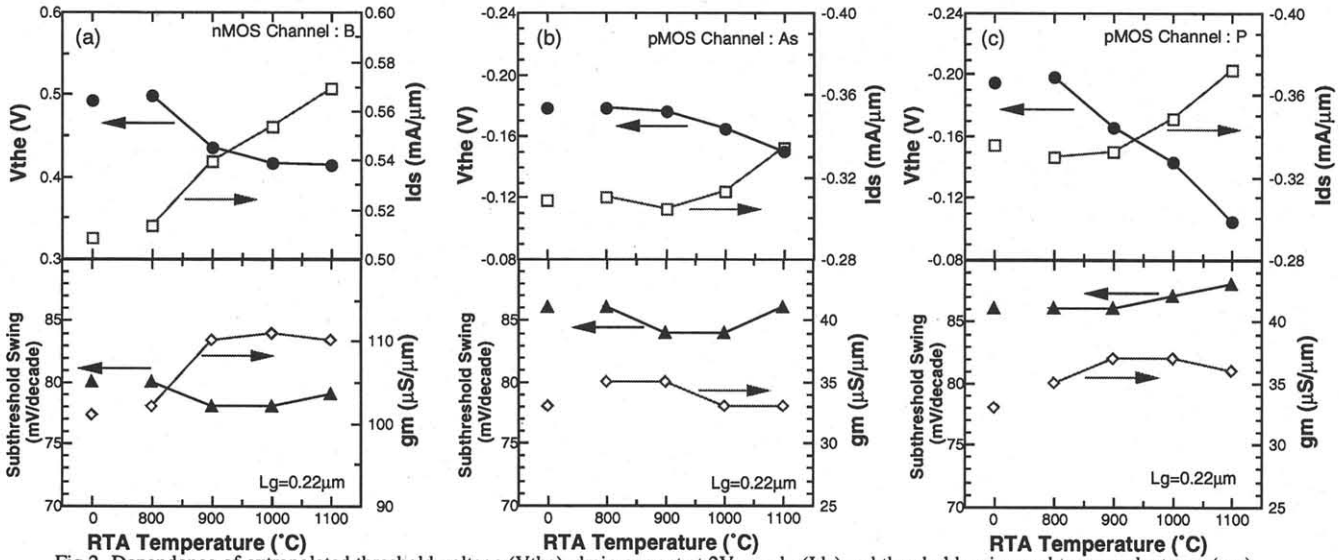

Fig.2 Dependence of extrapolated threshold voltage (Vthe), drain current at 2V supply (Ids), subthreshold swing and transconductance (gm) of 0.22 μm transistor upon the temperature of RTA before gate oxidation. (a) nMOS with B-channel, (b) pMOS with As-channel, (c) pMOS with P-channel. RTA at 0 °C means conventional process.

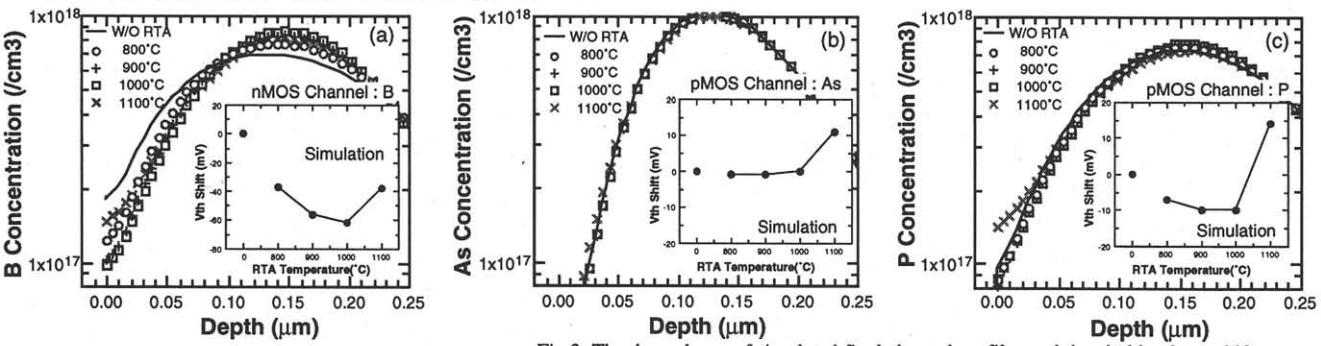

Fig.3 The dependence of simulated final channel profiles and threshold voltage shifts upon temperature of RTA before gate oxidation using point defect based diffusion model. (a) nMOS with B-channel, (b) pMOS with As-channel, (c) pMOS with P-channel.

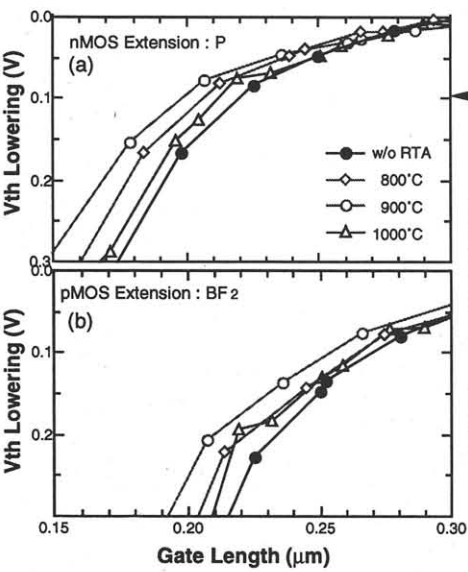

Fig.4 The dependence of short channel characteristics of threshold voltage on RTA temperature before TEOS deposition for formation of sidewall spacer. Vth lowering stands for difference from threshold voltage of transistor with 0.4 μm gate length. (a) nMOS P-extension, (b) pMOS BF_2-extension

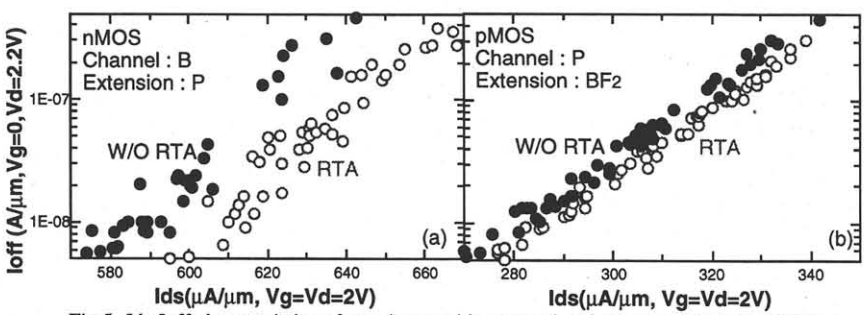

Fig.5 Ids-Ioff characteristics of transistors with conventional process and with additional RTA processes before gate oxidation and before TEOS deposition for sidewall spacer. (a) nMOS with B-channel and P-extension, (b) pMOS with P-channel and BF_2-extension