Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Hamamatsu, 1997, pp. 512-513

Uniform Si-SEG and Ti/SEG-Si Thickness Ratio Control for Ti-Salicided Sub-Quarter-Micron CMOS Devices

Hitoshi Wakabayashi, †Takeshi Andoh, Tohru Mogami, Toru Tatsumi, and Takemitsu Kunio

Microelectronics Research Laboratories and †ULSI Device Development Laboratories, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan
Tel:+81-427-79-6193, Fax:+81-427-71-0886, E-mail:waka@mel.cl.nec.co.jp

Introduction

Sub-quarter-micron CMOS devices require low-resistance self-aligned silicide (Salicide) on the poly-Si gates and source/drain (S/D) regions [1, 2]. Although $TiSi_2$ films generally have low resistivity and high process adaptability, it is difficult to form low-resistance and narrow $TiSi_2$ films on the narrow poly-Si lines [3]. It has been reported that low-resistance $TiSi_2$ films can be fabricated by the selective silicon deposition and subsequent pre-amorphization (SEDAM) process [4]. However, it is difficult to grow high-quality Si film formed by selective epitaxial growth (SEG), because SEG-Si film formation is very sensitive to the Si-surface condition. Thus, it is important to clarify the Si-SEG condition in order to form uniform and low-resistance $TiSi_2$ films with a low junction leakage current.

In this paper, the Si-SEG process is investigated in terms of the SEG-Si film quality on the S/D regions. The relationship between Ti/SEG-Si thickness ratio and $TiSi_2$ sheet resistance is also investigated to form a uniform and a low-resistance $TiSi_2$ film.

Experiments

The salicided CMOS devices were fabricated using the Ti-SEDAM process, as listed in Table 1. After the S/D formation with ion-implantation (I/I) and rapid thermal annealing (RTA), the SiO_2 film was etched by either the 'dry' or the 'wet' process. Then the thermal flushing and the Si-SEG were carried out by the cold-wall UHV-CVD system. That can selectively deposit Si films on both the n^+/p^+ poly-Si gate and the n^+/p^+ S/D regions with the same thickness and without severe dopant diffusion into the SEG-Si film [5]. After the Si-SEG, pre-amorphization As I/I was carried out into the SEG-Si film in order to enhance the Ti-silicidation on narrow Si lines. Then Ti film was deposited, and the 2-step RTA process was carried out to form the Ti-salicide film.

Results and Discussion

Figure 1 shows an SEM photo of a SEG-Si film surface with the 'dry' process. A large number of pits were observed in the SEG-Si films on S/D regions. In particular, the cross-sectional photo of one of these pits was observed by XTEM, as shown in Fig. 2. This XTEM photo shows that a pit grown during the Si-SEG process is generated from a very small region on the Si surface. In order to observe pit influence in S/D regions, junction leakage current between S/D and well regions was evaluated in Fig. 3. The reverse current of n^+/p junction with a lot of pits increases considerably with increasing Ti thickness. It can be easily speculated that this leakage current increase is caused by the shallower junction below the pit, as shown in Fig. 4. Therefore, it is necessary to eliminate the pits to form a low-leakage pn junction with $TiSi_2$ film.

To clarify the pit generation mechanism, impurity depth profile was observed. The carbon contamination layer ($\sim$ 2E19 cm^{-3}) is formed between SEG-Si film and Si substrate with the 'dry' process, as shown in Fig. 5. Therefore, it can be speculated that a pit bottom on the Si surface consists of carbon-contaminated layer which is generated by SiO_2 dry etching process in CHF_3 and O_2 gases and is not removed by the DHF dipping and the thermal flushing. In order to eliminate the pits, we carried out carbon-less 'wet' etching process. The carbon concentration in the 'wet' process is smaller than that in the 'dry' one between the SEG-Si and the Si substrate, as shown in Fig. 5. By using this clean process, no pits are observed in the SEG-Si film, as shown in Fig. 6.

Figure 7 shows the reverse current dependence on the S/D sheet resistance with the 'dry' or the 'wet' process for p^+/n and n^+/p junctions. The reverse current increases with decreasing the sheet resistance for the n^+/p junction with the 'dry' process, because the n^+/p-junction depth is shallower than the p^+/n one. In contrast, no reverse current increase is observed for both the p^+/n and the n^+/p junctions with the 'wet' process.

The stable formation of low-resistance silicide film on narrow n^+ and p^+ poly-Si lines is another key issue for CMOS devices fabrication. Figure 8 shows that the sheet-resistance dependence on the Ti/SEG-Si thickness ratio on n^+ and p^+ poly-Si. When the Ti/SEG-Si ratio is less than 1.0, the sheet resistance and their standard deviations are considerably small. In contrast, when the Ti/SEG-Si ratio is more than 1.0, the standard deviation values are very large. These large deviation values are caused by poor silicidation and agglomeration of $TiSi_2$ film, especially at the poly-Si line edge, as shown in Fig. 9. For a 0.75 Ti/SEG-Si ratio, the $TiSi_2$ film sheet-resistance values are lower than 6 $\Omega/\square$, and the standard deviations are sufficiently small, for n^+ and p^+ poly-Si electrodes down to the width of 0.14 μm, as shown in Fig. 10.

Finally, good I_D-V_D characteristics for 0.2 μm nMOSFET and pMOSFET are obtained, as shown in Fig. 11. Therefore, Si-SEG with the 'wet' process and salicide process with Ti/SEG-Si thickness ratio control are suitable for high-drivability sub-0.25 μm CMOS devices.

Conclusion

The Ti-salicide process for sub-quarter-micron CMOS devices was investigated. The number of pits in the SEG-Si film was suppressed by SiO_2 wet etching before the SEG-Si film formation. The good pn junction characteristics was achieved for uniform SEG-Si film with 'wet' process. Furthermore, when the Ti/SEG-Si thickness ratio was less than 1.0, the $TiSi_2$ sheet resistances and their standard deviations became considerably small ($\leq$ 6 $\Omega/\square$) on the 0.14 μm n^+ and p^+ poly-Si.

References

[1] H. Wakabayashi et al., Ext. Abst. SSDM, p. 622 (1994).
[2] T. Horiuchi et al., VLSI Symp. Tech. Dig., p. 121 (1994).
[3] Jerome B. Lasky et al., IEEE Trans. Electron Devices, vol. 38, No. 2, p. 262 (1993).
[4] T. Mogami et al., IEDM Tech. Dig., p. 687 (1994).
[5] T. Tatsumi et al., Ext. Abst. SSDM, p. 668 (1992).

Table 1: Salicide process flow with 'dry' and 'wet' processes.

processes	dry	wet
LOCOS formation and well & channel I/I gate and SiO_2 side wall formation SiO_2 deposition (10 nm) S/D I/I (As 30 keV, BF_2 20 keV) RTA (1000 $°C$ 10 sec in N_2)	⇓	⇓
SiO_2 dry etching in CHF_3 and O_2 gases **DHF dipping** **thermal flushing** (750 $°C$ 3 min) **Si-SEG** (650 $°C$)	⇓ ⇓	× ⇓
pre-amorphization As I/I Ti-silicidation metallization	⇓	⇓

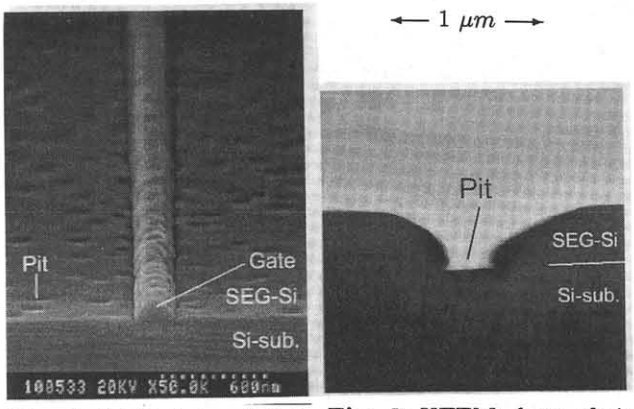

Fig. 1: SEM photo of SEG-Si film surface with 'dry' process for nMOSFET.

Fig. 2: XTEM photo of pit in Fig. 1.

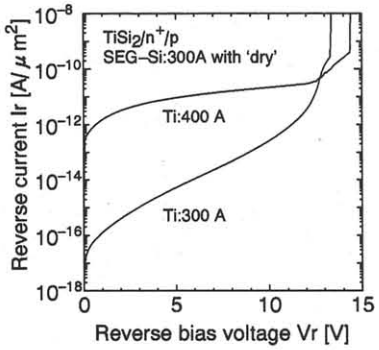

Fig. 3: Reverse current dependence on the Ti thickness for n^+/p junction with 'dry' process.

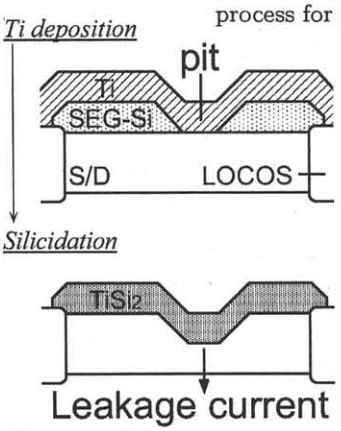

Fig. 4: Schematic images of leakage current origin caused by pit.

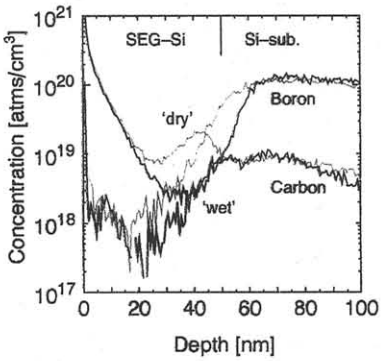

Fig. 5: SIMS depth profiles with 'dry' or 'wet' process.

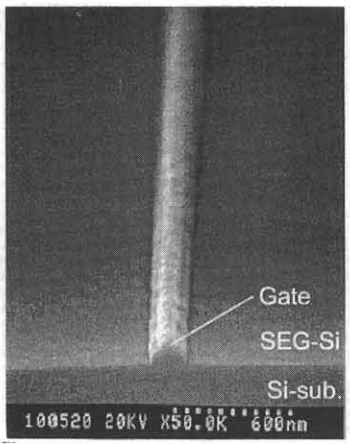

Fig. 6: SEM photo of SEG-Si film with 'wet' process for nMOSFET.

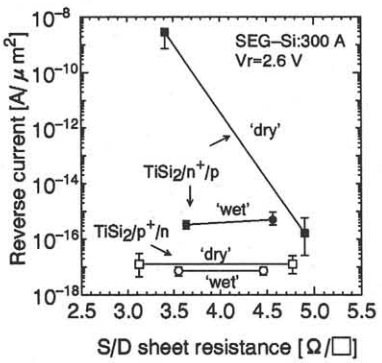

Fig. 7: Reverse current dependence on S/D sheet resistance with 'dry' or 'wet' process.

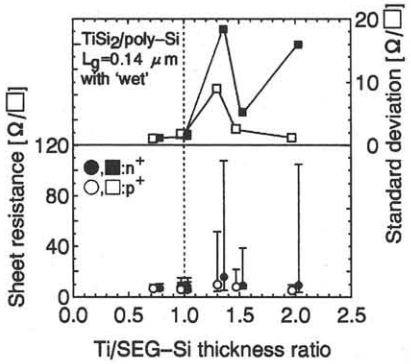

Fig. 8: Sheet resistance and standard deviation dependence on Ti/SEG-Si thickness ratio.

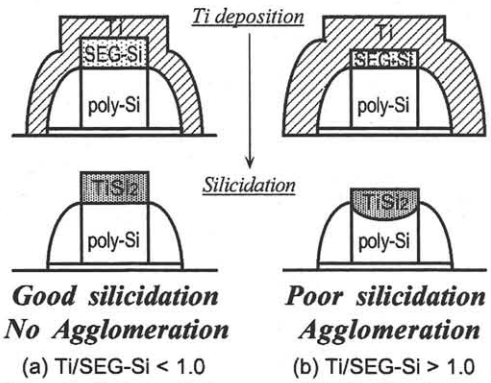

Fig. 9: Schematic images of $TiSi_2$ film formation on poly-Si gate for (a) Ti/SEG-Si < 1.0 and (b) Ti/SEG-Si > 1.0.

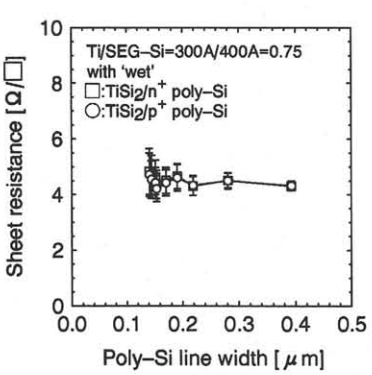

Fig. 10: Sheet resistance dependence on n^+ poly-Si and p^+ poly-Si line width.

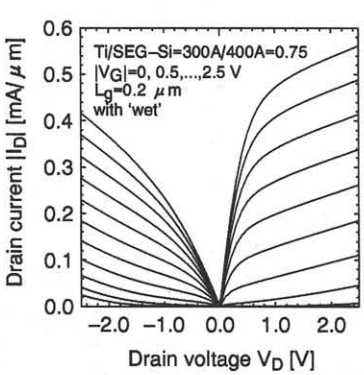

Fig. 11: I_D-V_D characteristics for nMOSFET and pMOSFET.