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Cell Transistor Design Using Self-Aligned Local Channel Implant(SALCI) for 4Gb DRAMs and Beyond

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1. Introduction

To meet the tight electrical performance requirement of cell transistors used in 4Gb DRAMs for low voltage operation, junction leakage current(I_J) caused by tunneling or traps, junction capacitance(C_J), and the threshold voltage (V_{TH}) should be controlled very carefully. As the channel length(L_G) of cell transistor is scaled down to less than 0.15μm, the substrate doping concentration(N_{SUB}) should be higher than $1\times10^{18}cm^{-3}$ to obtain the threshold voltage around 1.0V. However, critical physical limitations of using highly doped channel are imposed by abrupt increase in I_J and C_J at high $N_{SUB}(>1\times10^{18}cm^{-3})$ [1-2]. In this paper, we propose highly manufacturable self-aligned local channel implant (SALCI) method to obtain high doping in channel region for the threshold voltage control and low doping in source/drain regions to suppress I_J and C_J.

2. Fabrication Process

The main feature of the Self-Aligned Local Channel Implant(SALCI) method is that the channel implant and gate oxide growth are done with the reverse gate pattern, and then the gate region is filled with gate poly materials without additional mask steps. Fig. 1 shows the process steps of NMOS cell transistor using SALCI method. After STI(Shallow Trench Isolation) and well implant process, the wafer is deposited with 200Å of SiN, 500Å of SiO_2, and 2000Å of SiN layers sequentially. After the deposition step, SiN on the reverse gate region is etched and then filled with SiO_2 followed by CMP process. Then, channel implant and the gate oxide growth are performed on the gate region after the SiN over the gate region is removed. In the reverse gate region, the channel implant is prohibited by thick SiO_2. Fig. 2 shows the SEM cross section of the cell transistor after SiN gate pattern removal. So, the highly doped region($>1\times10^{18}$ cm^{-3}) is formed only beneath the gate oxide, and the source/drain regions remain unaffected. The gate region is filled with N+ poly followed by the CMP and SiO_2 etching process. After SiO_2 strip, spacer and S/D formations are applied sequentially.

3. Results and Discussion

Figs. 3 shows the TSUPREM simulation results of doping profiles of the cell transistors based on SALCI and conventional methods. In the channel region, the magnitude of the doping concentration for the conventional cell is higher than that of SALCI cell although they are implanted with the same amount of channel implant dose density. The channel doping difference between two methods is mainly due to the fact that the dopant out-diffusion during the thermal oxidation is enhanced by localized channel implant in SALCI cell transistors. So, in order to obtain identical V_{TH} for two cases, the channel implant dopant density should be increased for SALCI method. On the other hand, in the source/drain regions, the cell transistor with local channel implant shows much lower doping concentrations when compared with the conventional one. For the conventional cell transistor, source/drain junctions are formed with high substrate doping. For the cell transistors with SALCI method, the channel implant is strongly localized by reverse gate pattern so that the source/drain junction is formed with low substrate doping.

Figs. 4 and 5 show the simulated source/drain junction capacitance and leakage currents of cell transistors based on conventional and SALCI methods with respect to the junction voltage V_J and channel implant dose, respectively. The junction capacitance of cell transistors with local channel implant is reduced by 30% compared to that of the conventional ones. Due to reduced junction capacitance obtained with SALCI, C_S/C_B ratio is increased and we can obtain enlarged sensing margin and low V_{CC} operation margin without using increased cell capacitance. Meantime, junction leakage current of SALCI cell is reduced to 50% of that of conventional cells. Due to reduced doping in the junction region, junction leakage of SALCI cell transistors increases at a lower rate compared to that of conventional ones as the channel implant dose increases. Reduced junction leakage current due to low substrate doping in SALCI cells can provide increased data retention time and lowered standby power for DRAMs. Even for the sub-0.1μm cell transistors which require higher channel doping, we can successfully suppress the junction leakage current and capacitance by using SALCI method.

4. Conclusion

In conclusion, we proposed highly manufacturable self-aligned local channel implant for 4Gb DRAMs and beyond. By using SALCI method, we can eliminate the physical limitations of using highly doped channel imposed by junction capacitance and leakage current.

References

[1] M. Ono, et al., *IEEE Electron Devices*, pp. 1510-1521, 1995.
[2] H. Nakamura and T. Horiuchi, *VLSI Tech.*, pp.67-68, 1995.
[3] K. Noda, et al., *VLSI Tech.*, pp.19-20, 1994.

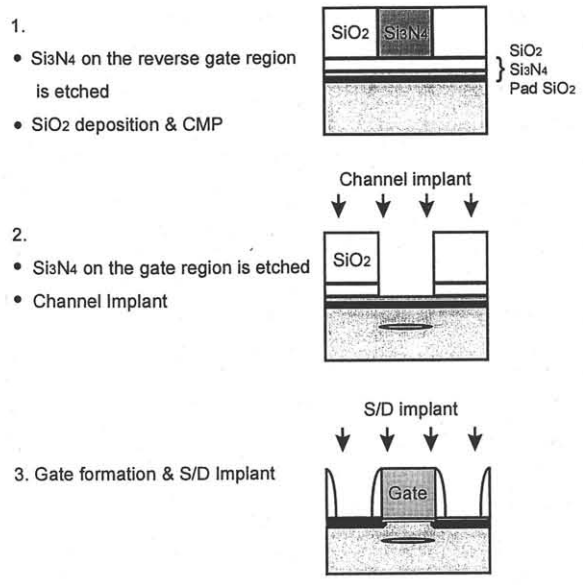


Fig. 1: Process steps of Self-Aligned Local Channel Implant Method.

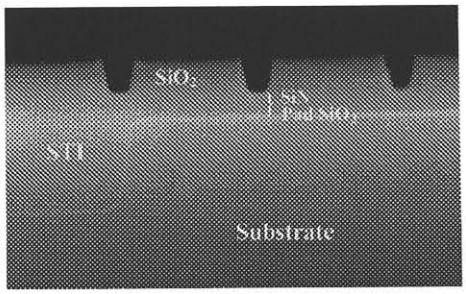


Fig. 2: The SEM cross section of the SALCI cell after SiN gate pattern removal.

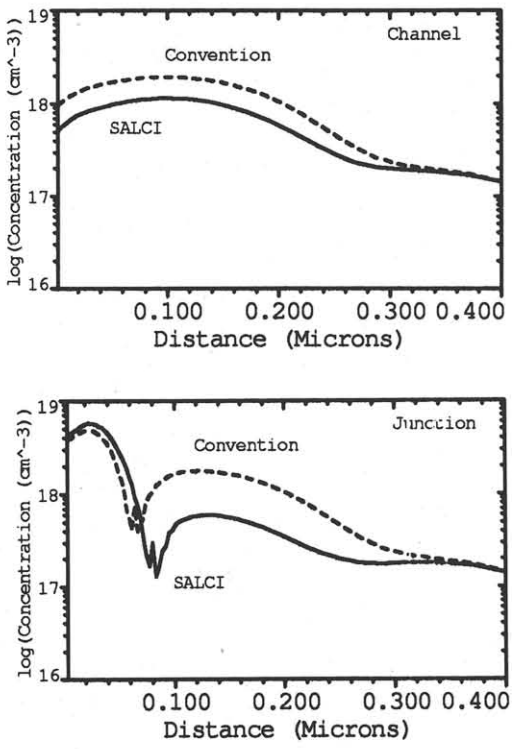
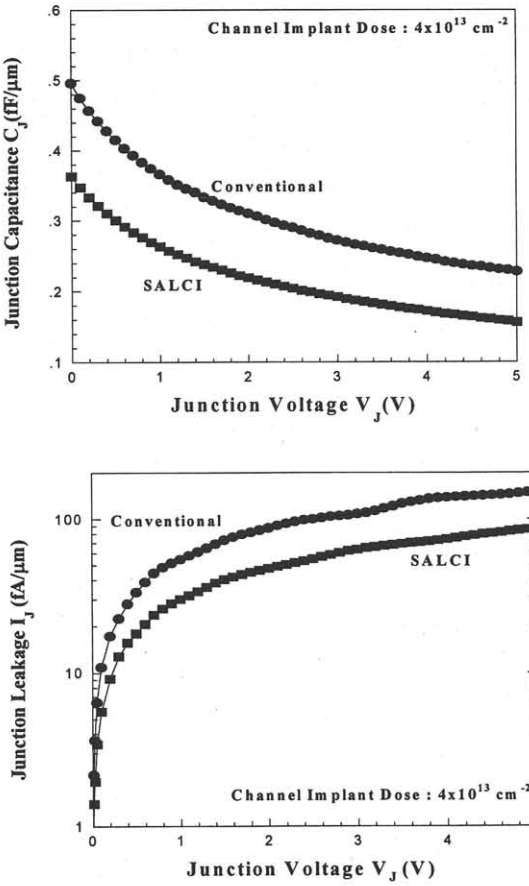
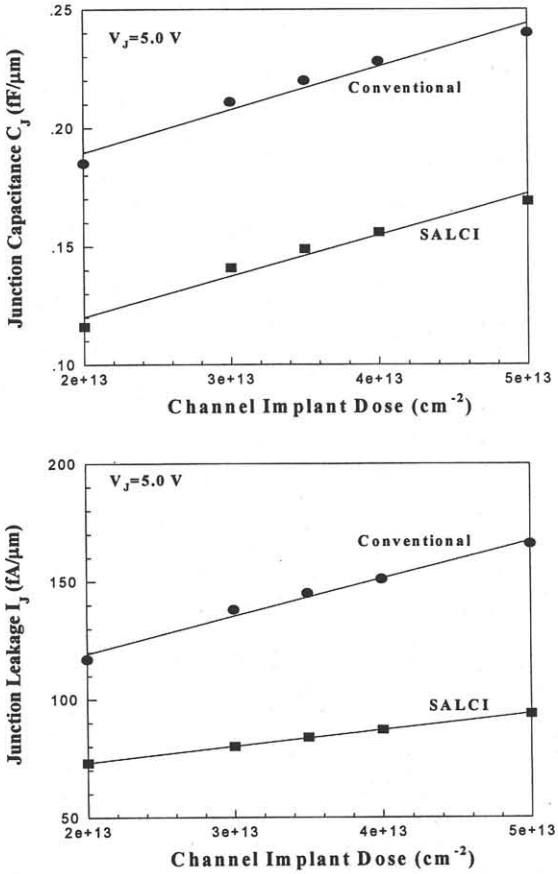


Fig. 3: The simulation results of channel and S/D junction doping profiles of SALCI and conventional cell transistors.



Figs. 4: Simulated source/drain C_J & I_J as a function of V_J in the source/drain regions with channel implant of $4\times10^{13}cm^{-2}$.



Figs. 5: Simulated source/drain C_J & I_J as a function of channel implant dose with V_J=5.0V.